



PONTIFICIA UNIVERSIDAD CATÓLICA DE CHILE
ESCUELA DE INGENIERÍA

ARM LINK ENHANCED MODULAR MULTILEVEL CONVERTER FOR LOW VOLTAGE AND VARIABLE FREQUENCY APPLICATIONS

RODRIGO IGNACIO AGUILAR VILLASECA

Thesis submitted to the Office of Research and Graduate Studies in
partial fulfillment of the requirements for the Degree of
Master of Science in Engineering

Advisor:

JAVIER EDUARDO PEREDA TORRES

Santiago de Chile, June 2023

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*To my family, mother, father,
siblings, and pets, who were always
there.*

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ABSTRACT

Modular Multilevel Converter has taken a lot of interest from research and industry due to all its benefits. Its modularity, scalability, waveforms quality and efficiency have shown clear advantages over other multilevel topologies, and make it ideal for medium and high voltage applications. Nevertheless, it is not exempt of challenges: its large number of capacitors require a complex control to balance the energy, besides needing a large space due to high capacitances. Due to this, the MMC is not considered for low voltage applications, where also the large number of semiconductors do not justify its cost. This work presents a deeper analysis and the validation of a proposed novel topology, named Arm Link Enhanced MMC (ALE-MMC). This extends the MMC to low voltage and variable frequency applications through the use of Dual Active Bridges (DAB) to allow power flow between Sub-Modules (SM) of the same leg. The new topology is presented and its operation is studied considering the suppression of the circulating current, showing that it is not necessary to use voltage measurements to work properly and the SM capacitance can be reduced. Next, all the issues to be considered due to the implementation of the DAB are studied. Emphasis is put on the rating currents and on the effects of variable frequency on the topology, with and without circulating current control. To validate the proposed scheme and the theoretical analysis carried out, a three-phase ALE-MMC is simulated to test its correct operation, evaluating its behavior in different scenarios and comparing it with the proposed scheme. Later, an experimental single phase ALE-MMC prototype is used to validate its operation in practice, also in different scenarios to be able to confirm the previous analysis. Finally, the results are discussed in addition to proposing improvements for future works with the converter.

Keywords: Modular Multilevel Converter, Dual Active Bridge, Low voltage variable speed drives, Circulating current suppression.

RESUMEN

El Conversor Multinivel Modular (MMC) ha tomado mucho interés por parte de la investigación y la industria debido a todos sus beneficios. Su modularidad, escalabilidad, calidad de formas de onda y eficiencias han mostrado claras ventajas sobre otras topologías multinivel, y lo hacen ideal para aplicaciones de medio y alto voltaje. Sin embargo, no está exento de desafíos: su gran cantidad de capacitores requiere un control complejo para balancear la energía, además de necesitar un gran espacio debido a las altas capacitancias. Debido a esto, el MMC no es considerado para aplicaciones de bajo voltaje, donde además el gran número de semiconductores no justifican su costo. Este trabajo presenta un análisis más profundo y la validación de una nueva topología propuesta, llamada Arm Link Enhanced MMC (ALE-MMC). Esta extiende el MMC a aplicaciones de bajo voltaje y de frecuencia variable mediante el uso de Dual Active Bridges (DAB) para permitir el flujo de potencia entre submódulos (SM) de una misma pierna. Se presenta la nueva topología y se estudia su operación considerando la supresión de la corriente circulante, mostrando que no se necesita emplear medición de voltaje para funcionar adecuadamente y la capacitancia del SM puede ser reducida. A continuación, se estudian todos los problemas a considerar debido a la implementación del DAB entre SMs. Se hace énfasis en la corriente que debe manejar y en los efectos de la frecuencia variable en la topología, con y sin control de corriente circulante. Para validar el esquema propuesto y el análisis teórico desarrollado, se simula el ALE-MMC trifásico para probar el correcto funcionamiento, evaluando su comportamiento ante distintos escenarios y comparando con el esquema propuesto. Seguido, se emplea un prototipo experimental del ALE-MMC monofásico para validar su operación en la práctica, también ante distintos escenarios para poder confirmar en análisis hecho. Finalmente, se comentan los resultados además de proponer mejoras para futuros trabajos con el conversor.

Palabras Claves: Conversor Multinivel Modular, Dual Active Bridge, Drives de bajo voltaje y frecuencia variable, Supresión de corriente circulante.

1. INTRODUCTION

The growing market of hybrid and electric vehicles (HEVs and EVs) is forcing both academy and industry to develop and research more reliable and improved power systems for traction purposes. The main topics on this research can be grouped in three: electric motor, energy storage (batteries) and power converters (power electronics) (Sarlioglu, Morris, Han, & Li, 2017).

EVs implement various electric motors in their design, but attention is put on the traction motor, since it is the crucial component that allows the vehicle to move. Permanent Magnet (PM) machine and its variants are widely used to achieve the traction, but there are also some vehicles which employ Induction Machines (IM) (Emadi, Lee, & Rajashekara, 2008). Main improvements involve stator and rotor design with ferrite magnets and new dispositions of the machine windings. In PMs the use of more powerful rare earth magnets and their physical distribution can improve the motor specifications and efficiency (Islam, Husain, Fardoun, & McLaughlin, 2009; Parsa & Toliyat, 2007)

Batteries define key specifications of the vehicle, such as cost, autonomy and acceleration, as it limits the maximum energy and peak power obtainable (Sarlioglu et al., 2017). Specific energy and energy density are the main targets of improvements, since the acceleration and autonomy depends directly on them. The higher these parameters, more space will be available for either more energy, power converter or user functions. Lithium-based batteries are the most used ones, and research and development mainly focus on its variants to improve the aforementioned parameters, as well as the drive-train efficiency (Williamson, Khaligh, Oh, & Emadi, 2005).

Power converters have various roles on HEVs and EVs, depending on their configurations. DC-DC converters are used to convert the DC battery voltage to low voltage levels (12 or 24 V), and also exists inverters for driving air-conditioning or service air pumps. Converters for the charging ports are also needed for the EVs to be charged with conventional grid (Onar, Kobayashi, Erb, & Khaligh, 2012; X. Cheng et al., 2014).

The inverter used to actuate the motor is usually called the variable speed drive. It allows to convert the batteries energy and use it in the AC motor to get mechanical power and thus, torque and traction. This speed drive also allows to control the regenerative braking, seizing the mechanical energy to recharge the batteries. Main improvement targets for all these converters are the efficiency, power density, specific power and the power rating.

The development of improved converters for electrical speed drives involves several challenges. Considering the amount of power the motor needs to operate, plus the losses of the power semiconductors, proper thermal management is required. This directly affects the power density and specific power, since the cooling systems are a great part of the converter and motor volume (Sarlioglu et al., 2017). Thermal dissipation also makes necessary to employ components that can withstand high temperatures, reducing the design flexibility.

Most research are focused on producing more efficient and faster power semiconductor devices, which helps to reduce the converter sizing in different aspects, but not many analyze the use of different topologies. The following section summarizes the state of the art of electrical speed drives, focusing on the different topologies that exist for different applications, contrasting their advantages and disadvantages.

1.1. Electrical speed drives: State of the art

As mentioned before, one of the main aspects to consider when designing electrical speed drives is their volume and weight. Also, issues like cost, impact on batteries, floating capacitors, isolated DC sources, fault-tolerance and charging and discharging speeds must also be taken into accounts when considering traction applications (Poorfakhraei, Narimani, & Emadi, 2021). Traditionally, the speed or motor drive was placed separately from the motor, being connected through long power wires. This produces economic and technical disadvantages, such as the need of electromagnetic interference (EMI) filters and lower power density.

In recent years, Integrated Motor Drives (IMD) have been proposed and used as a solution mainly for the low density problem of separated motor and speed drive. IMDs enclose both motor and speed drive in a single unit. This greatly increases the power density, and no long power wires are needed, thus lowering potential EMI and reducing general costs (Abebe et al., 2016). This single unit also allows to use a single cooling system for both semiconductors losses and motor heating. However, this makes the design of the cooling system more complex, as more heat must be cooled down in the system. This limits the power range of the IMD since at higher power ratings, losses and heat become larger.

Depending on the converter topology used, IMDs can be designed to be a single mounted unit, or a modular integrated unit. The latter allows to reduce the stress on semiconductors, more power density and rating and cost reductions. Topologies currently used will be covered in the next sub-sections.

1.1.1. Matrix converter

The matrix converter is an AC-AC converter that directly transforms the AC input voltage into an AC output voltage of the desired frequency, without a rectifying stage in between. Its configuration is shown in Fig. 1.1. It consists of nine bidirectional switches to perform the conversion.

An advantage of this topology is the free output frequency, making it ideal for wide speed range motors (Wheeler, Rodriguez, Clare, Empringham, & Weinstein, 2002). Other advantages are a small size as there is no DC-link voltage needed, bidirectional power flow and input power factor control.

However, the voltage transfer ratio is low compared to other topologies. It also needs extra circuitry for protection and a capacitive input filter (Klumpner, Nielsen, Boldea, & Blaabjerg, 2000). Costs are also higher as the total number of switching devices (and diodes) is 18 and they are in a non-conventional configuration, demanding

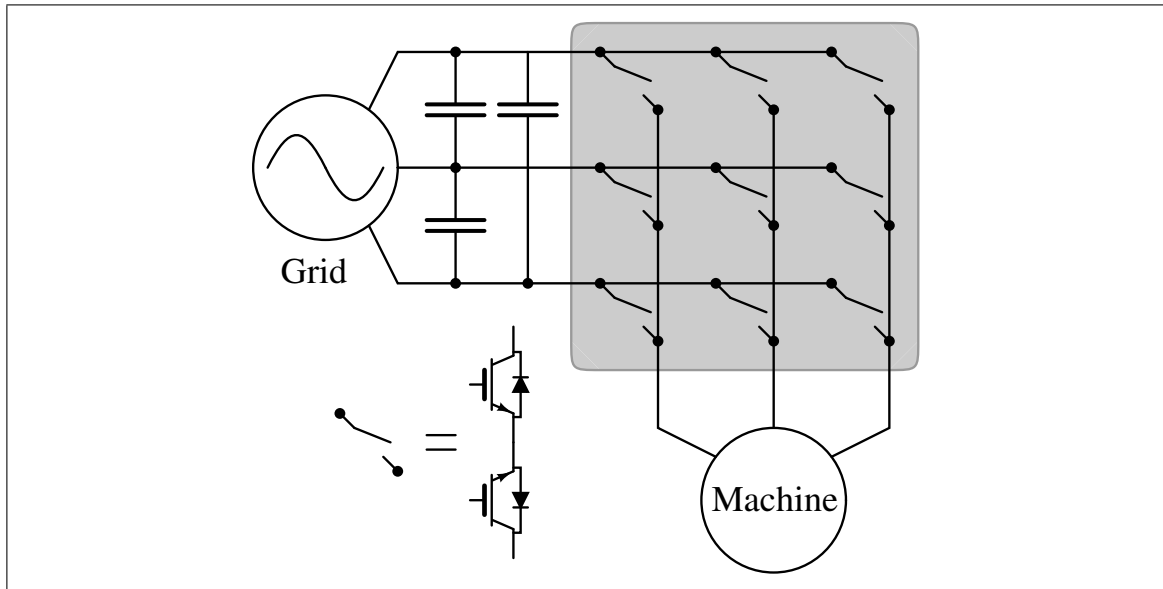


Figure 1.1. Matrix converter topology.

custom power modules. Besides this, the absence of a DC-link capacitor implies no input-output decoupling, meaning no ride-through capabilities (Simon, Mahlein, Muenzer, & Bruckmarm, 2002).

In EV applications, this topology has more advantages in electric powered trains that are connected to AC catenaries, but is not considered in battery-powered speed drives as it requires an AC input voltage. Thus, it is discarded for applications where a DC voltage is the only source of energy for traction.

1.1.2. Conventional two-level inverter

The two-level inverter is one of the oldest, most used and studied three-phase converters, making it a reliable topology for many applications. Its configuration is shown in Fig. 1.2.

Its simply configuration offers a great number of advantages. It also has a large variety of well-studied modulations, and is relatively easy to control, allowing to choose the best suited for the particular application. Bidirectional power flow is also available.

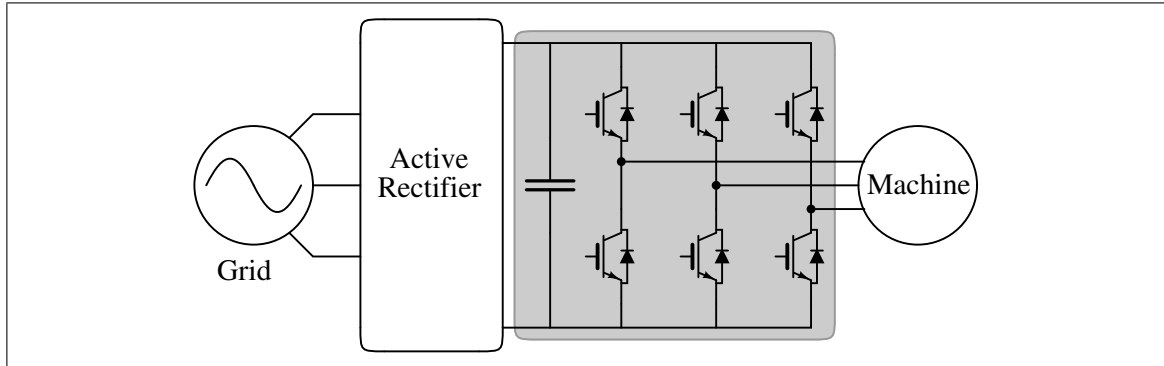


Figure 1.2. Conventional two-level converter topology.

As a extensively used converter, power modules are available in a wide range of power ratings, going from a hundred of Watts to MWs. Different semiconductor technologies are also available for these power modules, such as MOSFETs or IGBTs, with Si or SiC composition (Abebe et al., 2016).

Main drawbacks of this topology comes inherently from its operation (Poorfakhraei et al., 2021). Power semiconductor must withstand the whole DC-link voltage, increasing the rating of the devices and also the switching losses. Additionally, as only two voltage level are produced, high current THD is generated. This, in addition to potential EMI, produces mechanical vibrations, so the machine must endure these vibrations in order to be a reliable design. This limits the potential electric machines availability.

For EVs applications, even with the main drawbacks this converter is well-suited for electrical speed drives, since it can be fed easily with the battery voltage. Its market availability makes easy the hardware design of the converter, and the few components and low complexity make it a more inexpensive option compare to other topologies.

1.1.3. Multiphase full bridge converter

This converter is derived from the classic two-level inverter, and allows to control machines with higher number of phases. The topology is shown in Fig. 1.3.

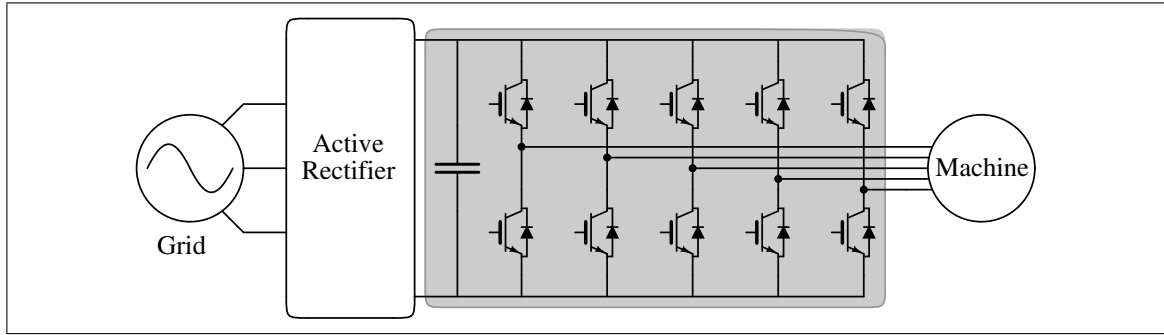


Figure 1.3. Multiphase full bridge converter.

In addition to control machines with higher number of phases, these converters increase the fault tolerance and allows power partitioning, that is desirable specially in IMDs (Abebe et al., 2016). It shares the same advantages as the three-phase two-level inverter, such as bidirectional power flow and availability in the market.

It also has the same drawbacks of the three-phase version: High current THD, wich translate into more losses in semiconductor and machine, and the limitation on the machine that must endure the mechanical vibrations.

In EVs application, multiphase converters are more considered in higher power rated machines where the need of multiphase is justified, such as electric marine propulsion (ships), large buses or heavy machinery.

1.2. Multilevel converters

The traditional two-level inverter, although it is available in a wide range of power ratings, can not be used directly in medium or high voltage applications. Standard switching devices used in this topology are MOSFETs and IGBTs (depending on the application), and their maximum blocking voltage only reaches a few kV, limiting their application to this range. (El-Hosainy, Hamed, Azazi, & El-Kholy, 2017). These limitations made grow the development and research of multilevel converter topologies as a solution for the limitations of the two-level converter (and similar), using these same

devices. These converters are mainly though for medium-voltage and grid-connected applications (Rodriguez, Lai, & Peng, 2002).

Together with higher voltage and power, multilevel converters offers other great advantages. The most remarkable is the improvement on the voltage and current waveforms, resulting in a higher power quality. They have lower THD with the same switching frequency, which translates into lower output filters, less torque vibrations (in machine applications) and lower losses, among others (Agrawal & Jain, 2017).

The different multilevel converters share similar challenges or disadvantages. The first and most obvious one is the higher number of switching devices in a more complex configuration, that reduces the system reliability. Depending on the topology, this can lead to non-equal power distribution in the devices, the need of extra circuitry and/or components (capacitors in particular) and an increased control complexity (Khoucha, Lagoun, Kheloui, & Benbouzid, 2011). The great number of components, in general, make these converters not suitable for low voltage applications, where the available space is an important restriction in many cases. Research is focused on optimize the utilization of the components while maintaining or improving the output waveforms, achieved either by modifying the structure or improving the control schemes.

Multilevel converters can be classified into various categories depending on their features. A generalized multilevel converter was also proposed from which other topologies can be derived (Peng, Qian, & Cao, 2010). However, only the most studied and considered ones will be mentioned in the next sub-sections. Three correspond to single DC source converters, which are the Neutral Point Clamped (NPC), Flying Capacitor (FC) and the Modular Multilevel Converter (MMC); and one corresponds to multiple DC sources, which is the Cascaded H-Bridge converter (CHB).

1.2.1. Neutral point clamped converter

NPC converter was shown in the previous section for the three-level case. It was introduced in 1981 (Nabae, Takahashi, & Akagi, 1981), and it was well received by industry and academy thanks to its relative high efficiency, specially for medium-voltage applications. A single leg of the NPC converter is shown in Fig. 1.4 (a) for the three-level case and in Fig. 1.4 (b) for the five-level case.

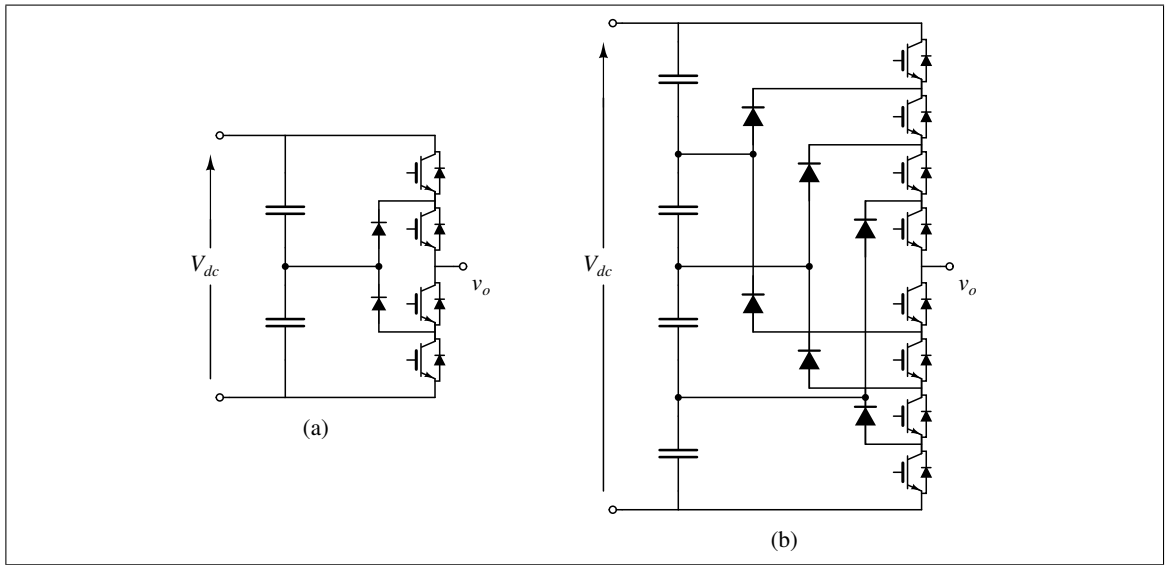


Figure 1.4. Single leg NPC topology: three-level configuration (a), and five-level configuration (b).

Its configuration splits the input DC voltage with series connected capacitors, and the output is “clamped” to these different voltage levels with the clamping diodes and the control of the switching devices. This way, different voltage levels can be generated at the output (Rodriguez, Bernet, Steimer, & Lizama, 2010), including the zero-voltage level, which effectively reduces the THD in the output current. Given that the capacitors splits the DC-link voltage, power semiconductors must withstand less blocking voltage so lower-rated voltage devices can be used and the switching losses are reduced (Abebe et al., 2016). This can simplify and reduce the size of the cooling system for the converter. The THD is reduced at the same switching frequency compared to the two-level converter

(Rodriguez et al., 2010). So this frequency can be reduced in order to lower the converter losses, or be used to reach higher fundamental frequencies, which is desirable in high speed drives.

Main drawbacks of this topology comes from the use of the capacitors for splitting the DC-link voltage. At high modulation index, a low-frequency ripple is produced on them (Celanovic & Boroyevich, 2000) and must withstand high temperatures, so the design must carefully choose these capacitors. In order to have a stable operation, the voltage on the capacitors must be correctly balanced by more complex control algorithms (Wang & Li, 2010). At higher number of levels (and capacitors), the balancing becomes more difficult. This, in practice, limits the NPC converter to three levels. However, research is constantly studying better modulation and balancing techniques (du Toit Mouton, 2002; Busquets-Monge, Bordonau, Boroyevich, & Somavilla, 2004). Also, it is not easily scalable to higher number of levels, as the topology greatly increases in complexity (Wang & Li, 2010). It does not have a modularity feature compared to other converters. It also has some unequal power distribution in some cases, but they can be fixed by modifying the configuration or adding extra components. In order to solve the balancing and power distribution problems, an Active NPC (ANPC) has been proposed, which replaces all diodes with active switches in order have a controllable path to the neutral point (Barbosa et al., 2005; Bruckner, Bernet, & Guldner, 2005).

Given its benefits, this converter is mostly used in Static VAR Compensators (SVC), medium voltage speed drives and HVDC systems interconnection (Du, Dekka, Wu, & Zargari, 2017b).

1.2.2. Flying capacitor converter

The Flying Capacitor topology was first proposed in 1992 (Meynard & Foch, 1992), and it is similar to the NPC but uses more capacitors in order to obtain the different voltage levels, requiring fewer devices. The configurations for the three- and four-level FC converter are shown in Fig. 1.5 (a) and (b).

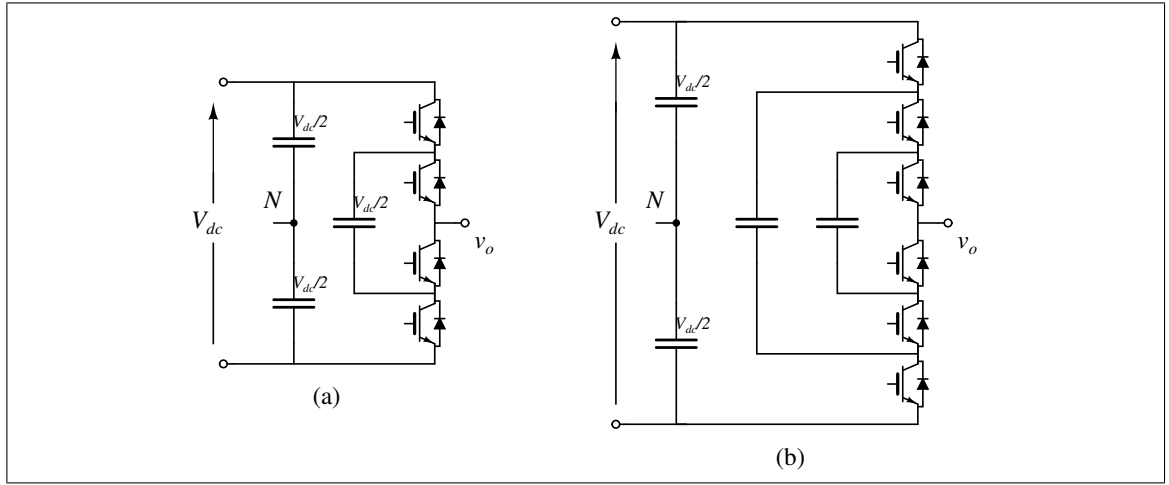


Figure 1.5. Single leg FC topology: three-level configuration (a), and four-level configuration (b).

FC uses fewer semi-conductor devices for the same levels compared to the NPC, which reduces the conduction losses. It has the advantage of having high modularity, which helps the replacing of modules and improves the large scale manufacturing, and has a high fault tolerance thanks to the energy stored in the capacitors (Du et al., 2017b). The other benefits are inherent to the multilevel waveforms, such as lower THD and better power quality.

Even with increased modularity, this converter has not been really considered for medium voltage and multilevel applications. The larger number of capacitors make this topology a lot more complex to control, since more and different voltages must be balanced for proper operation. Furthermore, having a large number of capacitors make this converter bulky, more expensive, and with a reduced lifetime compared to others (El-Hosainy et al., 2017). With a larger number of levels these problems worsen.

The applications of this topology are similar to the NPC, but its symmetrical loss distribution and low current ripple make attractive for high speed motor drives and active filter applications, but also for SVC and switched converters (Du et al., 2017b; El-Hosainy et al., 2017).

1.2.3. Cascaded H-Bridge

The two previous converters use a single DC source while relying on capacitors to generate the different voltage levels, having as a disadvantage the need of voltage balancing algorithms. Moreover, they cannot reach voltages higher than 6.6 kV without series connected devices, or higher than 13.8 kV with IGBT devices (Du et al., 2017b). The CHB converter topology uses multiple independent DC sources to generate different voltage levels so it can easily reach higher voltages, having the benefit of easy scalability. The converter is shown in Fig.1.6 (a), and the options for passive or active DC cells in Fig. 1.6 (b).

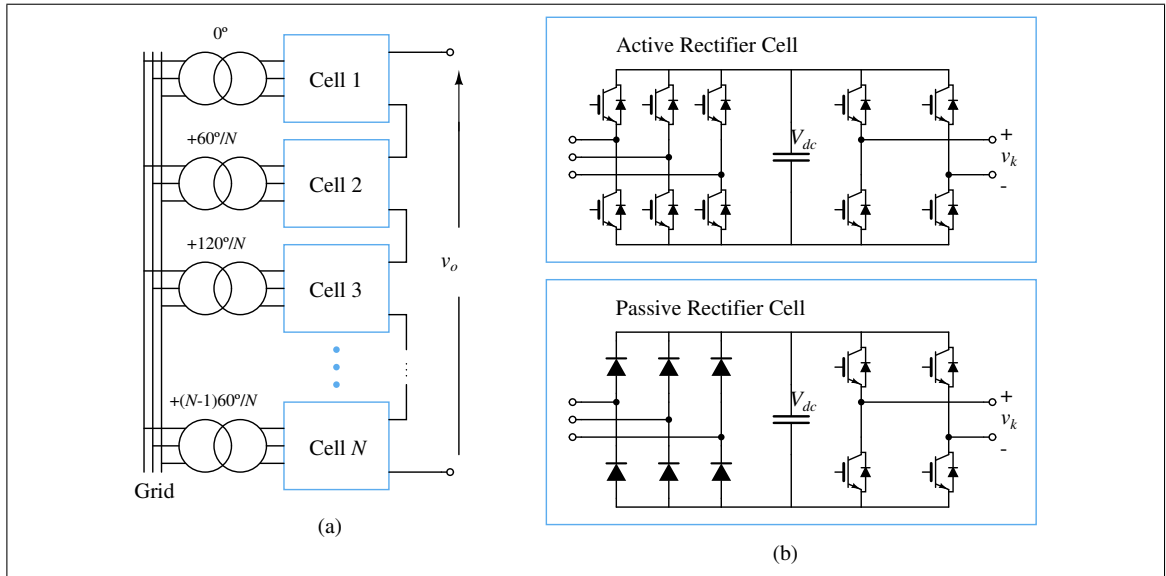


Figure 1.6. CHB configuration (a) and cell topologies (b).

CHB consist of series connected H-Bridges where each one has an independent DC source connected to its DC side. The DC sources are fed from the grid, and given that they generate harmonic distortion, it is necessary to use different transformer configurations to shift the phase of the harmonics and cancel the distortion out.

CHB offers various advantages. The first one is its modularity since same cells topologies are put in series. This make this topology easily scalable to theoretically any

desire number of levels, and a cell can be easily replaced in case of fault (El-Hosainy et al., 2017). The second one is that no voltage balancing control is needed if a proper modulation is implemented, as the DC sources are isolated from each other, simplifying the control algorithm needed. The fault tolerance is also high due to redundant power modules (Rodriguez et al., 2005).

The main disadvantage is the great number of isolated DC sources needed in order to generate the voltage levels. As said before, different transformer configuration are needed to shift the currents phase and avoid the harmonic distortion on the grid. This adds a lot of complexity in the construction of the converter, as well as increased costs (Du et al., 2017b).

An asymmetrical voltage version of this topology can reach higher number of levels with the same number of switching devices, and allows lower switching frequencies in higher DC voltage cells and thus higher efficiency (Pereda & Dixon, 2013, 2011). However, this implies different voltage-rated devices, uneven power distribution and a more complex cooling system, loosing the modularity property (Abu-Rub, Holtz, Rodriguez, & Baoming, 2010; Kouro et al., 2010). Basically all modulation techniques are available for this topology, making the control implementation flexible for the particular application. Given the main advantages, the CHB is used in more applications, such as motor drives, electric vehicle drives, power factor compensators (PFC), frequency link systems, and renewable energy sources interface (Du et al., 2017b).

1.2.4. Modular multilevel converter

Modular multilevel converter was first introduced in 2003 (Marquardt, Lesnicar, & Hildinger, 2002), and has received lot of attention from academy and industry due to its benefits. It has many of the advantages mentioned in the previous converters, and research is improving control methods in order to get the maximum performance from it. The topology is shown in Fig. 1.7 (a) for a single-phase, and with some of the cell options in (b).

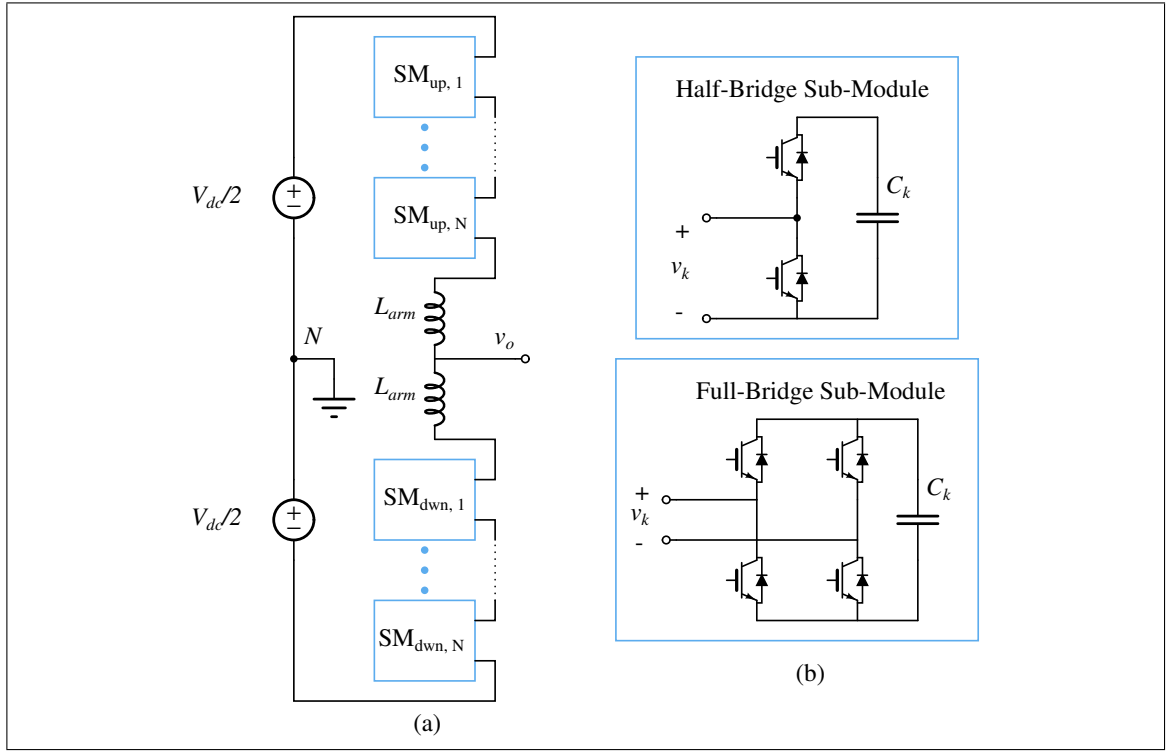


Figure 1.7. single-phase MMC topology (a) and SMs options (b).

The basic unit of the MMC correspond to a DC-AC converter connected to a capacitor on its DC side. This unit is called the Sub-Module (SM), and the capacitors allows to generate the different voltage levels (as in the NPC and FC converters). It can consist of any type of AC-DC converter, but the most used circuit is the Half-Bridge (Raju, Sreedevi, P Mandi, & Meera, 2019). The converter consist of two arms, where each one consist of stacked SMs (similar to the CHB). An arm inductor is used to limit some of the currents flowing through the arms.

As the name suggest, the main benefit is the modularity of the converter, since it is a simple arrange of SMs and their capacitors. It is scalable to a large number of levels without increasing its structure complexity or the need of auxiliary circuitry (in contrast with the NPC an FC). Other great advantage is that all modulation techniques can be used in this converter, where the Phase Shift PWM is highlighted, due to the benefits it produces.

However, the main drawbacks of this topology is the need of considerable high capacitances for the SMs. The capacitors must handle a power ripple that must be minimized for proper operation, which is achieved with both control algorithms and higher capacitance values. This translates into high control complexity due to the measurements system required and all the balancing algorithms involved (Akagi, 2010; Rohner, Bernet, Hiller, & Sommer, 2010). The result is a decreased lifetime and reliability, and the need of auxiliary control loops to balance the converter energies.

In general, the MMC owns many of the best advantages from the previously described converters, but it also has its challenges in order to get a robust and reliable operation. It is most applied for high- and medium-voltages applications of different areas, as it is flexible to work for various tasks (Du et al., 2017b).

The MMC operation and modeling will be detailed in Chapter 2, where its benefits and challenges will become clearer. For purposes of this thesis, the analysis will also focus on how the traditional configuration of the converter is not suitable for low voltage applications, neither variable frequency applications such as speed drives.

1.3. DC-DC converters

DC-DC converters are widely used in the low-voltage range for different applications, and also in different daily-use electronics devices. Figure 1.8 shows the most relevant DC-DC converters, classified by isolated and non-isolated topologies (Gorji, Sahebi, Ektesabi, & Rad, 2019).

Non-isolated topologies do not have galvanic isolation and do not have high step-up voltage gain ratios, but they are in general simpler configurations and have less weight compare to the isolated ones. On the other hand, isolated topologies are more complex and have the inherent problems of using a transformer, but they have higher conversion ratios. They also are more flexible to operate and in some cases they can have Zero-Voltage Switching (ZVS). Galvanic isolation allows to implement multiport topologies, so critical

and sensitive component can be safe in case of fault. Several and known control methods can be employed in these converters, such as the classical PID controller, sliding mode control, predictive control, among others, while there exist different modulation schemes depending on the topology used.

Bidirectional DC power flow is required and greatly beneficial in many DC systems involving different equipment and scenarios. Their applications include several areas such as energy storage systems, uninterruptible power supplies, renewable energy systems and DC distributions systems like in electric vehicles, marine and aerospace electric networks. In the particular case of electric mobility, weight, space and efficiency are basic requirements and target of improvement. Reliability and fault tolerance are also fundamental for implementing them in any system.

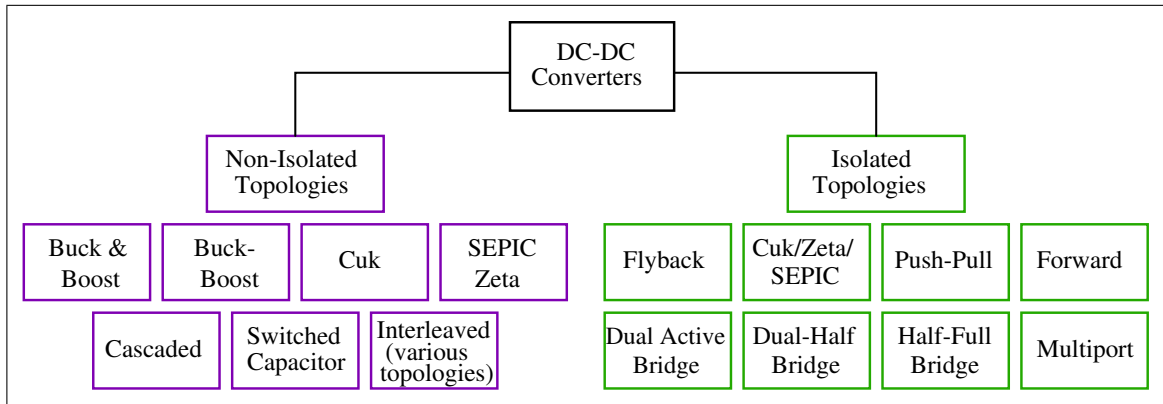


Figure 1.8. Classification of DC-DC converters: isolated and non-isolated topologies.

Among all the isolated DC-DC converters, the Dual Active Bridge is one of the most popular and preferred topologies in both academy and industry. This is due to three main reasons: auto-adjust bidirectional power flow, wide voltage conversion gain and ZVS capability (Mi, Bai, Wang, & Gargies, 2008). Also, using a high frequency transformer, size and weight of the converter can significantly be reduced. However, the DAB have problems with circulating currents that increase the losses of the converter, and ZVS is only reached under certain conditions (Shao, Chen, Wu, Zhang, & Sheng, 2019). Different

modulation and hardware modifications helps to solve these problems, and as a popular converter, lots of research has been made for this topology (Song, Chen, Pan, Du, & Zhang, 2019; Calderon et al., 2018).

Detailed analysis of the DAB is presented in Chapter 2, focused on the Single-Phase Shift (SPS) modulation, which is the simplest modulation technique for the converter. For the purpose of this thesis, the DAB will be used to transfer AC power between capacitors, where some undesirable effects appear due to the AC flowing power.

1.4. Original thesis contribution

The main contribution of this thesis is to analyze in more depth a new modular multilevel topology for bringing the multilevel conversion benefits to low voltage and variable frequency applications. Additionally, circulating current suppression and suitable operation at different speeds are proposed.

The studied topology is named Arm Link Enhanced Modular Multilevel Converter (ALE-MMC) and consist in a MMC with its upper and lower arm SMs interconnected or “linked” with a DAB converter. The main purpose is to manage the power fluctuation in the SMs capacitors with the DAB, reducing significantly the voltage ripple specially at low fundamental frequencies. This is thought for low voltage and variable frequency applications, where the number of SMs is relatively low and the DC-link voltage is under 1 kV. This solution allows to reduce size and complexity of the classical MMC, bringing the benefits of high power quality to the low voltage range, which the conventional two-level inverter does not provide.

All the advantages of the MMC for high voltage applications have been detailed previously, showing superiority over conventional two-level inverters. Thus, it is also of interest extending these benefits to lower voltage applications, specially due the high power quality provided (Perez, Bernet, Rodriguez, Kouro, & Lizana, 2015). This is also related to the availability of high-quality low-voltage semiconductor devices, which make

even more attractive the idea of multilevel conversion in the low-voltage range. Since the MMC is considered costly and complex for applications under hundred of kW, due to the number and size of the components and connections, it is little considered for these applications (Ashourloo, Zaman, Nasr, & Trescases, 2018).

Hence, this thesis analyzes in more detail the ALE-MMC topology, focusing on the control structure considering circulating currents and also the behavior of the key variables involved. This will allow a better sizing of the components, and also will give insights of how the converter should operate in different conditions. Finally, simulations and a low-scale experimental prototype are developed for verification and validation.

1.4.1. Objectives

A. General Objective

The general objectives of this thesis is:

- To design and analyze an ALE-MMC using its mathematical model so its challenges, sizing and control can be determined, in order to implement an operational simulation and develop a low-scale prototype for experimental testing, with the purpose of validating the converter as a viable solution for low-voltage variable frequency applications.

B. Specific objectives

The specific objectives for this work are listed below:

- Analyze the MMC and DAB original topologies.
- Evaluate the ALE-MMC to identify the coupling between the system variables and raise the challenges to overcome in the topology.
- Develop the control of the converter, evaluating its operation under different conditions.

- Simulate a three-phase ALE-MMC to validate theoretical analysis and guide the experimental tests.
- Develop a single-phase ALE-MMC prototype and its control to evaluate and validate the theoretical and simulated analysis.
- Analyze the results and propose future work to improve the topology and its general performance.

1.4.2. Hypothesis

The hypothesis are respect to the converter operation in low voltage and variable frequency scenario:

- **H₁**: The converter operates properly in terms of efficiency and performance (output voltage, input current, capacitor voltages and circulating currents) to the state-of-the-art MMCs, and a proper logic of circulating current suppression can increase the performance in the operating range.

1.4.3. Methodology

To answer the hypothesis, a mathematical model of the ALE-MMC has been developed, leaning on actual research that exist for both MMC and DAB converters. Together with the theoretical models, the required control schemes of the converter have been specified to achieve the objectives. After the models, three-phase simulations were implemented to help and partially confirm the theoretical analysis. Finally, a single-phase prototype has been built to verify the models and simulations and to validate the converter, measuring the relevant variables.

A. Evaluation methodology

To evaluate the converter, the general performance and quality of the output waveforms were analyzed on both simulation and experimental tests. A comparison between

simulation and experimental results was made in order to evaluate the precision. Specifically the losses or efficiency were analyzed for the performance, and the output current and voltage, as well as the SMs voltages were taken into account. As the ALE-MMC is intended to operate in the low voltage and variable frequency range, its performance was compared with a Two-Level inverter at simulation level, since it is a classical solution for electrical speed drives. Additionally, a topology and control scheme comparison was made between the classical MMC and the ALE-MMC, highlighting advantages and disadvantages.

B. Evaluation parameters

For both simulations and experimental tests, the following variables are parameters were considered and compared:

- Voltage ripple on the SMs capacitors.
- Output voltage and current quality, in terms of Total Harmonic Distortion (THD).
- Power and current managed by the DAB, and its transformer harmonic content (at simulation level).
- Circulating current amplitude and harmonic content.
- General efficiency and converter losses.

1.4.4. Thesis organization

Chapter 2 presents an analysis of the MMC topology. A mathematical model is developed bases on average modeling of the SMs, focusing mainly on the output and circulating current models. The different modulation techniques and control requirements for the different variables are presented, as well as the MMC advantages and challenges.

Chapter 3 presents the DAB converter operation and PWM modulation techniques, giving further details on the SPS modulation used in this work. Here will be mentioned the

benefits of using this particular topology for transfer power on the converter (in particular the ZVS), and the challenges it must face.

Chapter 4 introduces the ALE-MMC topology. The MMC side operation is briefly explained and a mathematical model is developed in order to determine how the DAB must operate to achieve low voltage ripple. Some design and behavior considerations are detailed regarding the new topology and the operating conditions. The control structure for the ALE-MMC is presented, including output, circulating and DAB current control schemes. A special emphasis is put on the circulating current suppression control, detailing the different effects it has on the converter performance and variables. Finally, a first estimation of the DAB power and current is made base on the circulating current control, which will help to size the DAB parameters.

Chapter 5 presents the simulation results for a three-phase converter driving mostly an apparent power of 5.6 kVA. Simulations at low and high fundamental frequencies are shown, as well as the performance contrast with and without circulating current suppression for different frequencies. Also, a special test with zero-frequency or DC output current is shown. Regarding the DAB operation, the harmonic spectrum of the DAB transformer is shown and compared with and without circulating current suppression control. Finally, losses estimations for the semi-conductor devices are presented with and without circulating control. The performance of the ALE-MMC is compared with a Two-Level inverter in similar conditions, where their losses estimations are compared, among other aspects.

Chapter 6 presents the experimental results for a low-scale single-phase converter prototype for verification and validation. A first test shows the converter operating without the DABs to demonstrate the effectiveness of the ALE-MMC main principle. Then, tests at different fundamental frequencies are performed, adding the circulating current suppression for comparison purposes. Frequency transients are also tested for studying the behavior. Finally, efficiency curves are shown in order to have an initial insight

of the converter performance, while discussing some considerations about the low-scale prototype.

Finally, **Chapter 7** contains the conclusions of the presented work reviewing the main results. The similarities and differences between theory, simulations and experiments are discussed. Finally, improvements and guidance for future works are presented in order to enhanced the converter performance.

2. MODULAR MULTILEVEL CONVERTER

As stated in the first chapter, other DC-AC multilevel topologies do not have the modularity and easy scalability property, except for the cascaded topology. The latter has a modular construction, allowing voltage and power scalability with the series connection of the power modules. They use low-voltage rated devices and offer fault-tolerance operation resulting in a high reliability. However, they require isolated DC-sources and phase-shifted transformers in order to work, limiting to some considerable extent the modularity property.

In this context, the introduction of the Modular Multilevel Converter meant a leading impact and development in the multilevel topologies. It keeps all the benefits of scalability and modularity as the cascaded topologies, but it does not require isolated DC-sources neither phase-shifted transformers to operate. Instead, it employs floating capacitors in its modules in order to generate a high-resolution waveform (Marquardt et al., 2002).

As a promising topology, the MMC generated an intense interest in the industry for different areas, while the academia constantly focuses on improving different aspects of the converter. Its applications commonly cover medium-voltage motor drives, power transmission systems such as High Voltage DC (HVDC) transmission and Multi-terminal systems, and also power quality improvement (Martinez-Rodrigo, Ramirez, Rey-Boue, De Pablo, & Herrero-de Lucas, 2017). Despite the benefits, specially at medium- and high-voltage, still the MMC is subject to various challenges before operating it correctly (Rohner et al., 2010).

2.1. Topology

The basic unit of the MMC are the Sub-Modules (SMs). A SM consist of a DC-AC converter with a capacitor on its DC side, being the Half-Bridge the most used and the one that will be analyzed in this work, shown in Figure 2.1(b). In some cases, other DC-AC

converters are used such as the Full-Bridge topology. The series connection of these SMs form a stack, with N_{SM} the number of SMs contained in the stack.

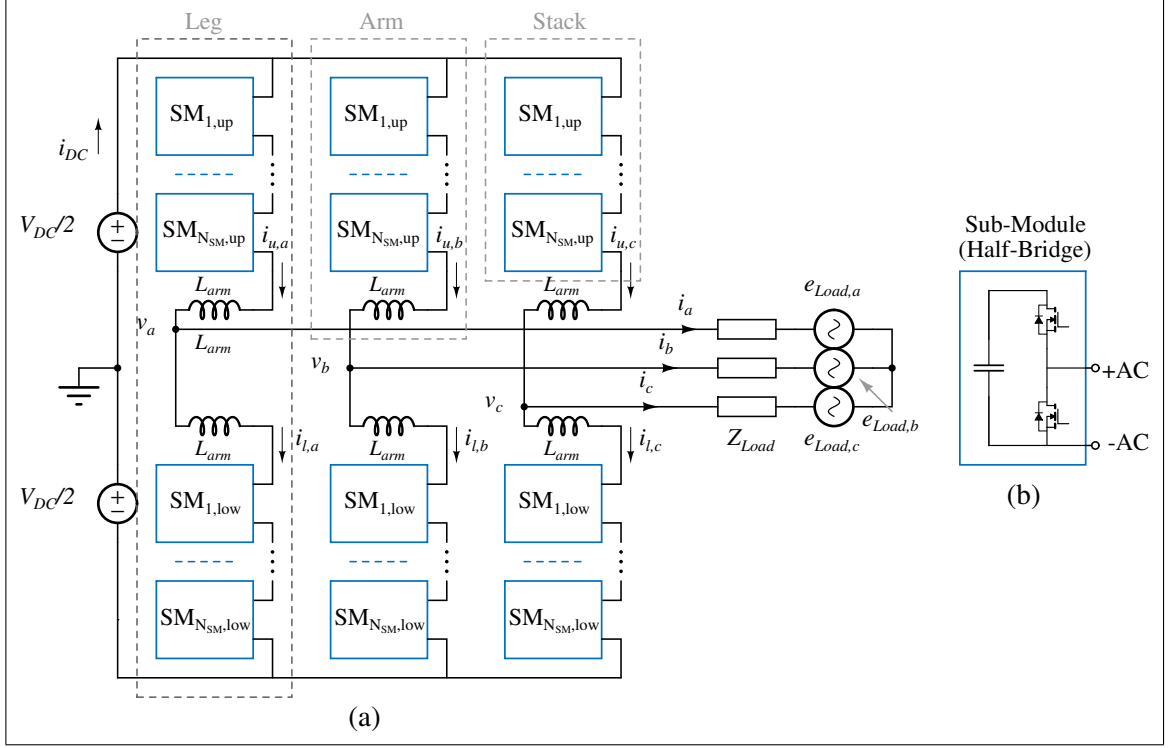


Figure 2.1. (a) Three-phase MMC topology and (b) Half-Bridge Sub-Module.

A three-phase MMC is shown in Figure 2.1(a). The DC link voltage V_{DC} is connected to the positive and negative nodes of a converter leg, and the AC system is connected to the mid-point of the same. A converter leg consists of two arms: an upper (sub-index u) and a lower (sub-index l) arm. The upper arm is connected to the positive bar of the DC link and to the AC system; while the lower arm is connected to the negative bar. Each arm consist of a SMs stack (or simply, a stack) and an inductor L_{arm} connected in series. The arm inductor is connected to the AC output of the leg.

Figure 2.1(a) shows clearly the modularity property of the MMC, and the scalability property is easily intuited. Given the basic structure, the nomenclature is introduced. V_{DC} and i_{DC} represent the DC link voltage and current, respectively. $x \in \{a, b, c\}$ represents

each of the phases, so v_x represents the output voltage of phase x . $i_{u,x}$ and $i_{l,x}$ are the upper and lower arm currents of phase x , respectively, and i_x is the output current of phase x . Z_{Load} is the equivalent output load, which includes R_{Load} and L_{Load} , while $e_{Load,x}$ is the load voltage in phase x . Finally, N_{SM} is the number of sub-modules in a stack.

The function of the series connected SMs is to add (or subtract) a voltage step or level to the respective output voltage phase. The ideal or nominal voltage on each SM is $\frac{V_{DC}}{N_{SM}}$. Given the modular structure, same or similar modulation techniques from the cascaded converters can be employed. As said previously, the structure of the MMC implies several technical challenges in order to operate properly. Most of them are related to the use of capacitors: SM voltage control, SM voltage ripple, circulating currents pre-charging process and the fault tolerance (Du et al., 2017b). Some of them will be explained with better detail in the following sections.

2.2. Modeling and Equations

There are several ways to model the behavior of the MMC, some with higher or lower level of detail. The choose of which modeling method is to be used depends on the main objective of the research. There are models which fits better to analyze current stress on critical components, and some other are better to see the converter behavior in transients periods or against faulty environments (Sharifabadi, Harnefors, Nee, Norrga, & Teodorescu, 2016b).

This section will describe an averaging modeling method which focuses on the general dynamics of the converter. This method provides a good start point or model to be used in the tuning of the main or primary controls, such as the output and circulating current controllers, which will be explained later. It is also useful to investigate power-related topics in the converter and/or the whole system where it is operating in. This is where secondary or tertiary controls are involved. However, it does not enter in specifics details of the SMs, so their voltage, semi-conductors losses and other variables are ignored.

The main simplification of this model is the replacement of the upper and lower SMs stacks with voltage sources. Figure 2.2 illustrates the simplified model and the schematic used for the modeling. Here, n_{dc} is the midpoint of DC-link voltage and n_{ac} is the star point connection of the load. As can be seen, the SMs stacks of each phase are replaced with ideal voltage sources $v_{u,x}$ and $v_{l,x}$, which represent the modulated voltages of the stacks given by:

$$\begin{aligned} v_{u,x} &= \frac{V_{DC}}{2} + m_{u,x} \frac{V_{DC}}{2} \\ v_{l,x} &= \frac{V_{DC}}{2} + m_{l,x} \frac{V_{DC}}{2} \end{aligned} \quad (2.1)$$

where $m_{u,x}, m_{l,x} \in [-1, 1]$ are the modulation signals for the upper and lower stacks, respectively.

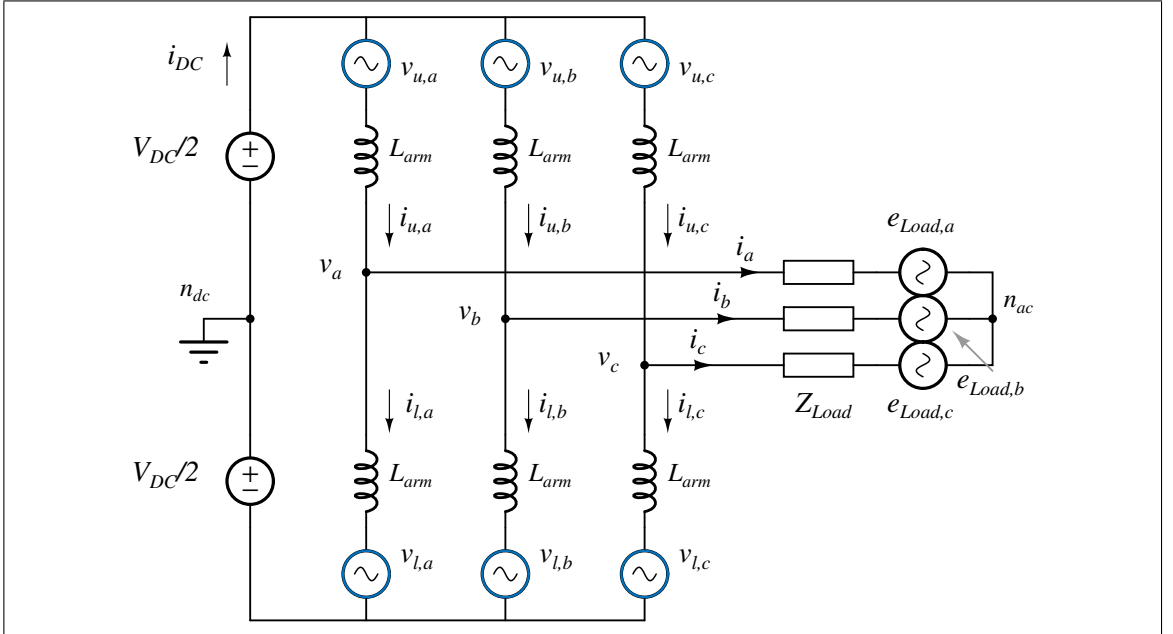


Figure 2.2. Simplified Model of the MMC for averaging modeling.

In order to have a better understanding of the converter, a linear transformation is used to introduce new terms. These terms will help to decouple the equations of the converter and are convenient for describing the operation. The first terms are related to the current,

being the linear transformation as follows:

$$\begin{bmatrix} i_x \\ i_{z,x} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{u,x} \\ i_{l,x} \end{bmatrix} \quad (2.2)$$

The first term of the left-hand side corresponds to the AC-side current, or the output current, which can be directly obtained by using Kirchhoff laws in Figure 2.2. The second term from the left-hand side can be interpreted as the average current flowing through the converter leg. This current is called the circulating current of the converter leg, and contains DC or AC components that flow through the leg without affecting the output current. This current has a lot of relevance since affects the general performance of the converter, and is also related to the voltage of the SMs capacitors.

The inverse transformation of equation (2.2) current terms is as follows:

$$\begin{bmatrix} i_{u,x} \\ i_{l,x} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & 1 \\ -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} i_x \\ i_{z,x} \end{bmatrix} \quad (2.3)$$

Equation (2.3) shows that the circulating current $i_{z,x}$ flows through both upper and lower arms in the same direction, meanwhile half of the output current flows through the arms but in opposite direction, which then are added at the AC-output.

On the other hand, there is also a linear transform regarding the upper and lower stack voltages:

$$\begin{bmatrix} e_x \\ e_{z,x} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{u,x} \\ v_{l,x} \end{bmatrix} \quad (2.4)$$

Here, e_x can be interpreted as the leg inner EMF (electromotive force) that drives the output current i_x . In the same way, $e_{z,x}$ can be interpreted as the mean voltage of the upper and lower stacks, that suppresses the circulating current $i_{z,x}$. The inverse transformation is as follows:

$$\begin{bmatrix} v_{u,x} \\ v_{l,x} \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} e_x \\ e_{z,x} \end{bmatrix} \quad (2.5)$$

As said before, equations (2.2) and (2.4) allow to decouple the currents of the converter, ease the understanding of the converter and shows how different variables can be controlled. Figure 2.3 shows the path of these currents in the converter, where can be seen how the circulating currents flow through the legs without being involved in the output current.

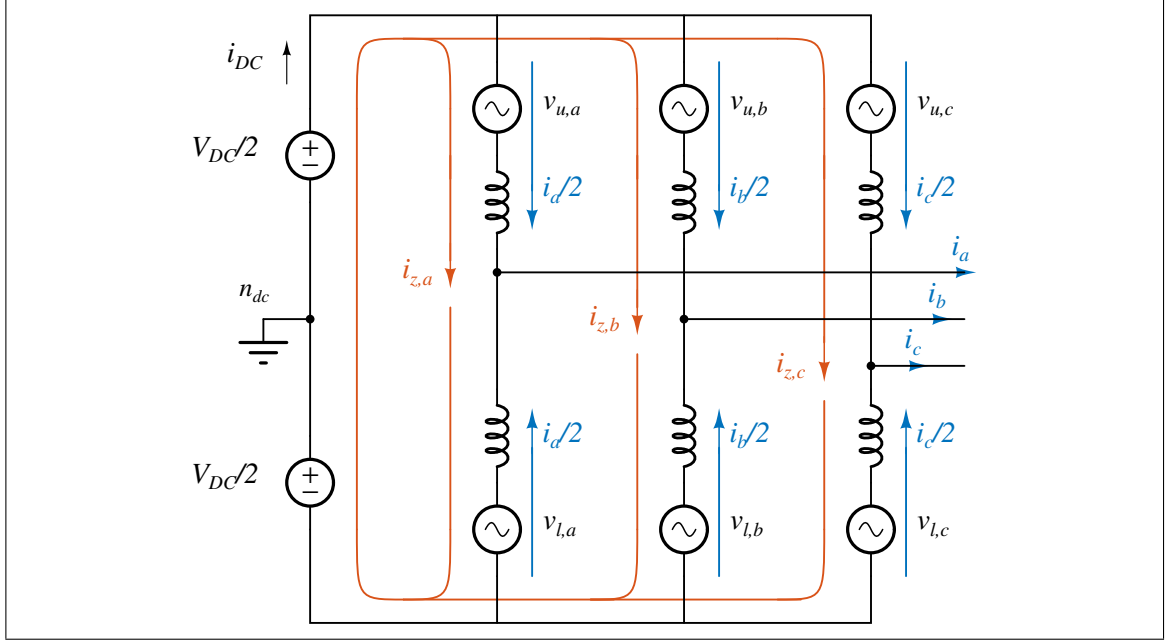


Figure 2.3. Path of the decoupled currents in the converter with the linear transformation.

2.2.1. Output Current Equation

With the decoupled terms introduced, the model and its equations can be determined. Taking Figure 2.2 as reference, applying Kirchhoff voltage law from the DC-link midpoint, passing through the upper arm of any leg, and ending in the star-point connection of the load, the following equation is obtained:

$$\frac{V_{DC}}{2} = v_{u,x} + L_{arm} \frac{di_{u,x}}{dt} + R_{arm} i_{u,x} + L_{Load} \frac{di_x}{dt} + R_{Load} i_x + e_{Load,x} + v_{cm} \quad (2.6)$$

Here, R_{arm} is the equivalent series resistance of the arm inductor L_{arm} , and v_{cm} is the common mode voltage defined as the difference between the star-point voltage v_{nac} and the DC-link midpoint v_{nac} ($v_{cm} = v_{nac} - v_{nac}$). In a similar way, the voltage law passing through the lower arm yields

$$\frac{V_{DC}}{2} = v_{l,x} + L_{arm} \frac{di_{u,x}}{dt} + R_{arm} i_{u,x} - L_{Load} \frac{di_x}{dt} - R_{Load} i_x - e_{Load,x} - v_{cm} \quad (2.7)$$

Combining equations (2.6) and (2.7), and using the linear transformations in (2.2) and (2.4), the equation governing the converter output currents is obtained:

$$\left(\frac{L_{arm} + 2L_{Load}}{R_{arm} + 2R_{Load}} \right) \frac{d}{dt} i_x + i_x = \frac{2}{R_{arm} + 2R_{Load}} (e_x - e_{Load,x} - v_{cm}) \quad (2.8)$$

Equation (2.8) indicates that the output current can be considered as a first order system with time constant $\tau_{i_x} = \frac{L_{arm} + 2L_{Load}}{R_{arm} + 2R_{Load}}$. As stated before, the output current can be controlled with the inner EMF of the phase leg e_x , which depends on the modulated voltage of the upper and lower SMs stacks.

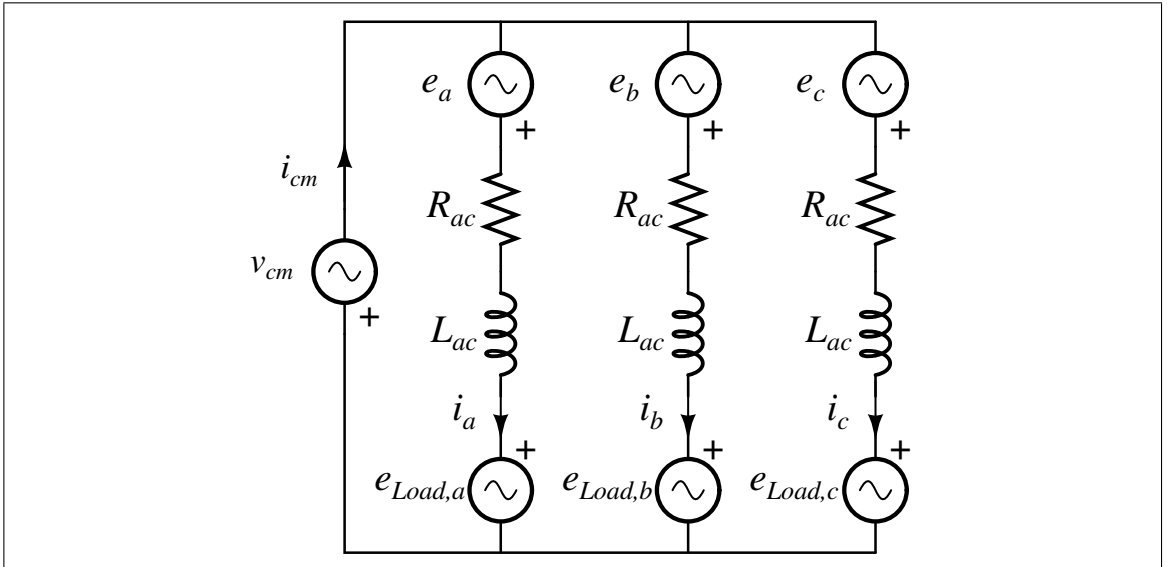


Figure 2.4. Equivalent circuit of the decoupled AC-side of the MMC.

Figure 2.4 illustrate the equivalent circuit of the decoupled AC-part of the converter. $L_{ac} = \frac{L_{arm}}{2} + L_{Load}$ is the equivalent AC inductance, which includes its equivalent AC series resistance $R_{ac} = \frac{R_{arm}}{2} + R_{Load}$. v_{cm} represents the common-mode voltages, which drives the common-mode current i_{cm} . In ideal operation where the neutral point of the load is not connected, $i_{cm} = 0$, and if the output voltages v_x are perfectly balanced, then $v_{cm} = 0$. However, due to parasitic effects on the systems there may exist an impedance that will allow a path for i_{cm} to flow. In these cases, if $v_{cm} \neq 0$ (which is usually the case) then $i_{cm} \neq 0$, meaning that there will be a parasitic current flowing in the system.

2.2.2. Circulating Current Equation

Using Kirchhoff voltage law for a loop comprising the DC-link and a phase leg yields:

$$V_{DC} = v_{u,x} + L_{arm} \frac{di_{u,x}}{dt} + i_{u,x} R_{arm} + L_{arm} \frac{di_{l,x}}{dt} + i_{l,x} R_{arm} + v_{l,x} \quad (2.9)$$

Using the linear transformation in equations (2.2) and (2.4) in equation (2.9) the circulating current equation is obtained:

$$\frac{L_{arm}}{R_{arm}} \frac{d}{dt} i_{z,x} + i_{z,x} = \frac{1}{R_{arm}} \left(\frac{V_{DC}}{2} - e_{z,x} \right) \quad (2.10)$$

Similar to the output current case, the circulating current equation can also be considered a first order system with time constant $\tau_z = \frac{L_{arm}}{R_{arm}}$. This current can be controlled with the mean inner voltage $e_{z,x}$ of the upper and lower stacks. It is notice that there is a constant voltage term $\frac{V_{DC}}{2}$ in the circulating current equation. Thus, the average DC voltage of $e_{z,x}$ must be this value in order to suppress it. This value is normally achieved as can be inferred from equation (2.1) and using (2.4), meaning that the right-hand side of the equation is zero. However, in reality this actually depends on how well the SMs capacitors are balanced.

The decoupled equivalent circuit for the circulating current can be obtained from the circulating current equation, shown in Figure 2.5.

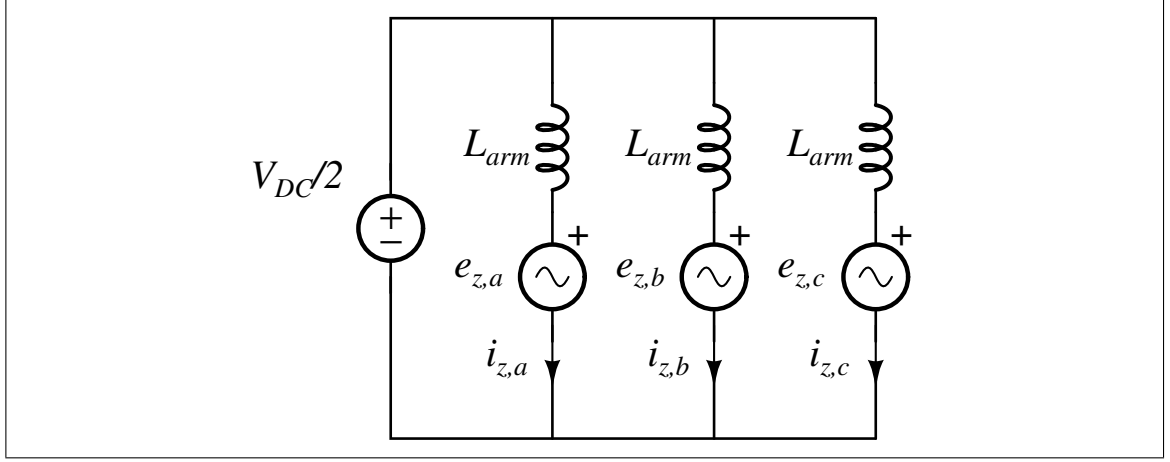


Figure 2.5. Equivalent circuit of the decoupled circulating current side of the MMC.

From Figure 2.2, using Kirchhoff current law at the DC positive node yields (similar can be made with the negative pole):

$$i_{DC} = i_{u,a} + i_{u,b} + i_{u,c} \quad (2.11)$$

Considering the relation for $i_{u,x}$ in equation (2.3), the DC current can be written as:

$$i_{DC} = \sum_{x=a,b,c} i_{z,x} + \frac{1}{2} \sum_{x=a,b,c} i_x \quad (2.12)$$

In normal operation the output currents are balanced implying that the second term in equation (2.12) is zero. Hence, the DC source current is the sum of the circulating currents of the three phases. Assuming no losses in the converter and recalling that the currents are balanced the output power is constant and consequently the input power is constant too. Thus, the DC-link current i_{DC} must be constant in normal operation. As the three legs are equal, the DC component of the circulating currents are assumed to be equal:

$$i_{z,x,DC} = \frac{i_{DC}}{3} \quad (2.13)$$

where $i_{z,x,DC}$ is the DC part of the circulating current for phase x .

An important detail of this model of the circulating current is that it only shows two driving voltages: the DC-link voltage and the mean stack voltage $e_{z,x}$. This is because the model replaces the SMs stacks with ideal voltage sources. However, in the real converter the SMs capacitors have voltage variations around their nominal DC voltage due to the currents flowing through the arms. This generates a voltage difference between the upper and lower stacks that drives an AC part of the circulating current, an effect not explicit in this model. This part of the circulating current tends to balance the SMs capacitors in some measure, but also increases the current stress on the devices. Thus, the circulating current can have both AC and DC components, which will be explained in the next subsection.

2.2.3. Power equations

The three-phase output power of a converter is expressed as:

$$P_o = \frac{3}{2} V_o I_o \cos(\varphi) \quad (2.14)$$

where P_o is the output power, V_o the peak phase-to-neutral voltage, I_o the peak phase current and φ the load angle. The modulated output voltage of a phase can be expressed as:

$$v_x = V_o \cos(\omega_0 t + \phi_x) \quad (2.15)$$

where ω_0 is the fundamental frequency of the converter and ϕ_x the phase angle. Accordingly, the output current is

$$i_x = I_o \cos(\omega_0 t - \varphi + \phi_x) \quad (2.16)$$

Now, the power balance between the AC and DC-side yields:

$$\frac{3}{2} V_o I_o \cos(\varphi) = V_{DC} I_{DC} \quad (2.17)$$

But the peak output voltage can be expressed in terms of the modulation index $\hat{m}_o$ and the DC-link voltage:

$$V_o = \frac{V_{DC}}{2} \hat{m}_o \quad (2.18)$$

So, replacing this in equation (2.17) gives the following relation:

$$3I_o\hat{m}_o\cos(\varphi) = 4I_{DC} \quad (2.19)$$

which are common equations for any three-phase converter.

Now, considering the nature and structure of the MMC, the arms voltage and currents are determined in order to analyze their power, specially in the SMs stacks. Recalling equation (2.1), the stacks voltages can be expressed in terms of the output modulating signal and other known variables. Here, $\hat{m}_o\cos(\omega_0t + \phi_x) = -m_{u,x} = m_{l,x}$.

$$\begin{aligned} v_{u,x} &= \frac{V_{DC}}{2} - \frac{V_{DC}}{2}\hat{m}_o\cos(\omega_0t + \phi_x) = \frac{V_{DC}}{2} - V_o\cos(\omega_0t + \phi_x) \\ v_{l,x} &= \frac{V_{DC}}{2} + \frac{V_{DC}}{2}\hat{m}_o\cos(\omega_0t + \phi_x) = \frac{V_{DC}}{2} + V_o\cos(\omega_0t + \phi_x) \end{aligned} \quad (2.20)$$

Each arm provides a DC voltage and a AC voltage for the converter output voltage. The arm currents, as stated in equation (2.3) carry half of the output current in opposite directions, and the circulating current. As seen in equation (2.13), the DC part of the circulating current is one third of the DC current in normal operation. Hence:

$$\begin{aligned} i_{u,x} &= \frac{I_{DC}}{3} + \frac{i_x}{2} = \frac{I_{DC}}{3} + \frac{I_o}{2}\cos(\omega_0t - \varphi + \phi_x) \\ i_{l,x} &= \frac{I_{DC}}{3} - \frac{i_x}{2} = \frac{I_{DC}}{3} - \frac{I_o}{2}\cos(\omega_0t - \varphi + \phi_x) \end{aligned} \quad (2.21)$$

With equations (2.20) and (2.21), the power exchange between SMs stacks can be determined. This is useful since it determines the average voltage ripple of the SMs capacitors. Multiplying the upper and lower modulated voltages with their respective currents, and using equations (2.18) and (2.19), the following is obtained:

$$\begin{aligned} p_{u,x} &= \frac{V_{DC}I_o}{8} \left[2\cos(\omega_0t - \varphi) - \hat{m}_o^2\cos(\omega_0t)\cos(\varphi) - \hat{m}_o\cos(2\omega_0t - \varphi) \right] \\ p_{l,x} &= \frac{V_{DC}I_o}{8} \left[-2\cos(\omega_0t - \varphi) + \hat{m}_o^2\cos(\omega_0t)\cos(\varphi) - \hat{m}_o\cos(2\omega_0t - \varphi) \right] \end{aligned} \quad (2.22)$$

$p_{u,x}$ and $p_{l,x}$ are the instantaneous power in the upper and lower SMs stacks, respectively. The first thing to notice is that there is no constant term in these powers, which means that

there is no energy accumulation in the SMs stacks (Ilves, Norrga, Harnefors, & Nee, 2014). Second, there are two fundamental frequency power oscillations which have opposite signs in the expressions for the upper and lower arms. This means that there is power fluctuating back and forth between the upper and the lower arm of a leg at the fundamental frequency.

Finally, there is a second-harmonic power term that has the same sign in both expressions, which represents power exchange with the entire phase leg. As in every converter, this second-harmonic power oscillation is also present in the MMC, and they normally cancel out with the other phases so there is not voltage ripple in the DC-link (Sharifabadi et al., 2016b). Now considering the real converter structure, all these power oscillations must be absorbed by the SMs capacitors, resulting in a voltage ripple around their nominal DC value. Due to this oscillations high capacitance is required in the SMs, increasing the size and cost of the MMC. To have the ripple in an acceptable value, dedicated control and balancing algorithms are used to reduce its amplitude, involving higher control complexity..

A last point about the power oscillations and voltage ripple, is that it generates a voltage difference between the upper and lower stacks, as said in the previous subsection. This voltage difference drives an AC component of the circulating current, at even harmonics of the fundamental frequency, a phenomenon not explicit in the previous model. For these reasons, the circulating current is usually modeled as:

$$i_{z,x} = \frac{I_{DC}}{3} + I_{2,z} \sin(2\omega_0 t + \phi_{2,zx}) + \sum_{n=2}^{\infty} I_{2n,z} \sin(2n\omega_0 t + \phi_{2n,zx}) \quad (2.23)$$

where $I_{j,z}$ is the amplitude of the j -th current harmonic and $\phi_{j,zx}$ its phase displacement for leg x . Normally, the second harmonic is the most significant one, and further harmonics are usually neglected. Even if these harmonics do not appear in the model, they still can be controlled with the mean voltage of the upper and lower arms $e_{z,x}$. This current can be either suppressed for reducing the current stress (Pan et al., 2018), or injected in order to reduce the voltage ripple (Pou et al., 2015).

2.3. Modulation and Switching Techniques

In order to synthesize a voltage signal at the output of any converter, this is, a reference voltage, different commutation methods are employed in the switching devices. Unlike the two-level inverters, cascaded topologies have more dc-voltages in their structure, allowing different switching techniques to commutate the devices (Du, Dekka, Wu, & Zargari, 2017a). The most popular methods make use of the Pulse-Width Modulation (PWM), existing different variants for this. Other methods do rely in simpler logic, and other do specific optimization to improve different aspects of the converter.

Most of the modulation schemes are based on using two modulating signals for one phase. As expressed in equation (2.1), an upper modulating signal is used to modulate a voltage in the upper stack, represented by $m_{u,x}$, and another for the lower stack, represented by $m_{l,x}$. The following subsection describes some of the modulations techniques used for the MMC.

2.3.1. Phase-Shifted Carrier PWM

The Phase-Shifted Carrier modulation (or PS-PWM) is one of the most considered and used multi-level modulation techniques (Du et al., 2017a), illustrated in Figure 2.6 for $N_{SM} = 4$. In its basic form, it allows to generate $N_{SM} + 1$ levels on the output voltage waveform. It consists of N_{SM} triangular carrier signals which are shifted an angle of $\frac{360^\circ}{N_{SM}}$ with respect to each other. All the carriers have full amplitude and the same frequency f_{sw} , and each carrier has a SM associated to it.

From the figure, the carrier signals are compared to $m_{u,x}$ to switch the upper stack SMs, and compared to $m_{l,x}$ for the lower stack SMs. The first carrier is for the first SM of both stacks and so on. In every voltage level, there is a SM commutating, so the equivalent output switching frequency is equal to $N_{SM} \cdot f_{sw}$

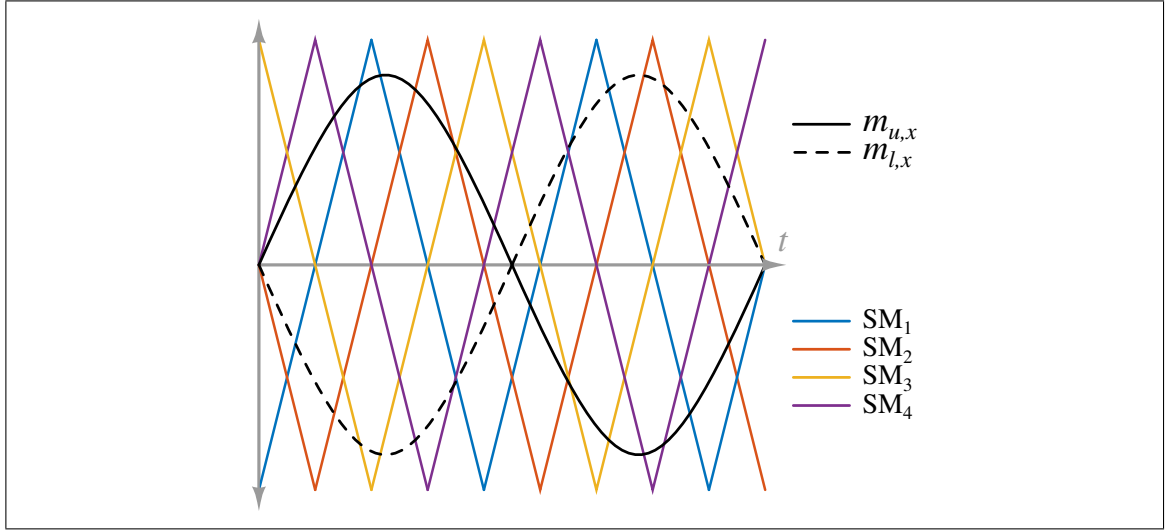


Figure 2.6. Phase-Shifted Carrier Modulation scheme.

In the PS-PWM, all the SMs are always performing a switching cycle independently of the modulating signals amplitude. Since all the carriers have the same amplitude and frequency, the dissipated power is distributed equally in all the SMs (B. Li et al., 2015). This advantage allows to use a simpler cooling method for the converter. Moreover, a consequence of this modulation is a natural balancing of the SMs capacitors, helping the algorithms to balance their voltage, which is the main reason why to choose it. However, it is not enough on its own and additional control must always be used to maintain in a stable level the capacitors voltage (Adam et al., 2010).

A variation of this method introduces separated carriers for the lower SM stack. These new carriers have a displacement angle θ_d with respect to the upper ones, depending on if N_{SM} is even or odd. This displacement angle allows to increase the output voltage levels to $2N_{SM} + 1$, so is highly considered since it can increase the number of levels at low cost. However, the use of the displacement angles directly affects the harmonic characteristics of both the SMs voltage ripple and the circulating current (B. Li et al., 2015). There is a trade-off between the output voltage and the circulating current harmonics. For minimum output voltage harmonics ($2N_{SM} + 1$ levels), $\theta_d = 0$ if N_{SM} is odd and $\theta_d = \frac{\pi}{N_{SM}}$ if N_{SM} is even. On the other hand, for circulating current without switching harmonics (and

$N_{SM} + 1$ levels), $\theta_d = \frac{\pi}{N_{SM}}$ if N_{SM} is odd and $\theta_d = 0$ if N_{SM} is even. (Q. Cheng, Wang, & Wang, 2020). Commonly, the higher voltage of levels is preferred over lower harmonics on the circulating currents.

2.3.2. Level-Shifted Carrier PWM

As the name suggest, the Level-Shifted Carrier modulation (or LS-PWM) employs N_{SM} carriers which are vertically shifted with respect to each other. This means that each one has a fixed offset level. In order to cover the whole range of the modulated voltage, the carriers do not have full amplitude, but they have the same frequency. There are three different method to arrange the carriers. The basic one in called Phase Disposition (PD), where all carriers have the same phase and they only differ in the level offset, illustrated in Figure 2.7. Another one, the Phase opposition disposition (POD), the carriers below

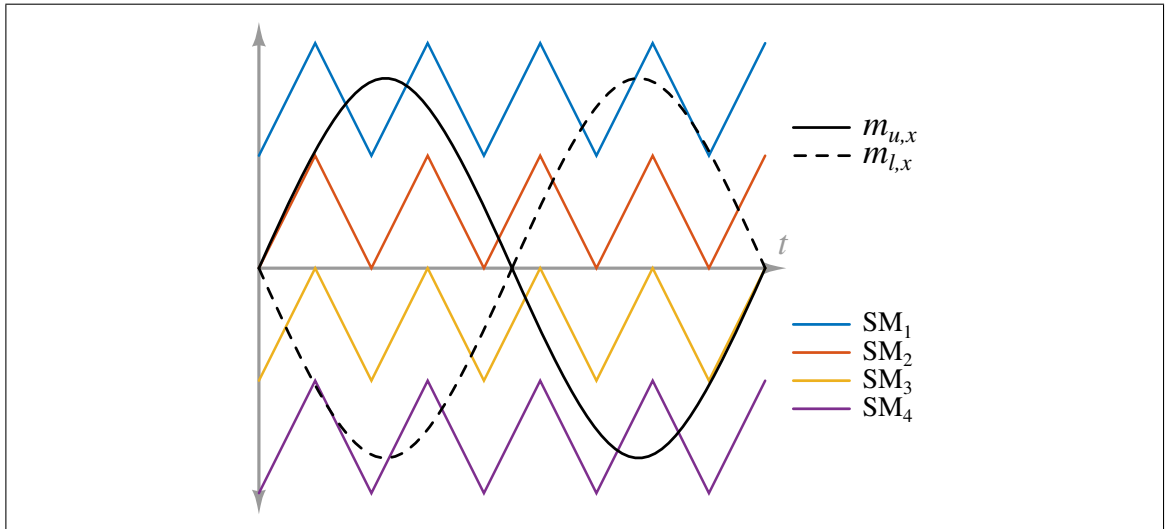


Figure 2.7. Level-Shifted Carrier Modulation scheme. Phase disposition case.

the zero level are shifted by 180° with respect to the ones above the zero level. Finally, the Alternative phase opposition disposition (APOD), alternates a phase of 0° and 180° so adjacent carriers will be in anti-phase.

Contrary to the PS-PWM, not all the SMs may be performing a switching cycle, since the commutation depends on the modulating signal amplitude. Consequently, the power losses are not evenly distributed in the converter SMs as well as the voltage ripple (Solas et al., 2013), but as an advantage, the switching losses are greatly reduced. The SMs associated with carriers close to the zero level must withstand a heavier work, since they are more prone to commute or being in "close" state for longer periods of time. For the same reason, the equivalent switching frequency is lower compared to the PS-PWM case. To achieve the same equivalent switching frequency as the case with PS-PWM, the LS-PWM carriers frequency must be multiplied by the number of SMs, but this translates into an increase of the switching losses.

The issue of the unevenly distributed losses, which also affects the balancing of the capacitors, can be addressed by employing algorithms that select which SMs will turn on or off, depending on the power dissipation and their capacitor voltage (Mei, Shen, Xiao, Tolbert, & Zheng, 2014). This is called the SMs sorting algorithm. This way, each SM is not associated with a specific carrier, and the choice of which SM must be enabled or disabled is based on the current state of the converter.

These balancing and sorting algorithms methods do exist in every modulation technique and may vary depending on the nature of the switching nature of the modulation. However, all have the objective of increase the performance of the converter, specially to improve the voltage balancing of the capacitors.

2.3.3. Nearest Level Control

The Nearest Level Control (NLC) is not a carrier-based modulation like the previous ones. Its concept is simpler and it consists on "sampling" the reference voltage signal at a high enough frequency and approximate the voltage level with the nearest level available (Meshram & Borghate, 2015).

A method to obtain the output voltage is to normalize the reference voltage with respect to the DC link voltage, times the number of SMs in the stack. Then, the value is rounded to the nearest integer (with the $\text{round}(x)$ function), and the result will give the number of SMs to be turned on in the stack (Du et al., 2017a). Figure 2.8 illustrate the concept for an upper stack modulation for $N_{SM} = 8$.

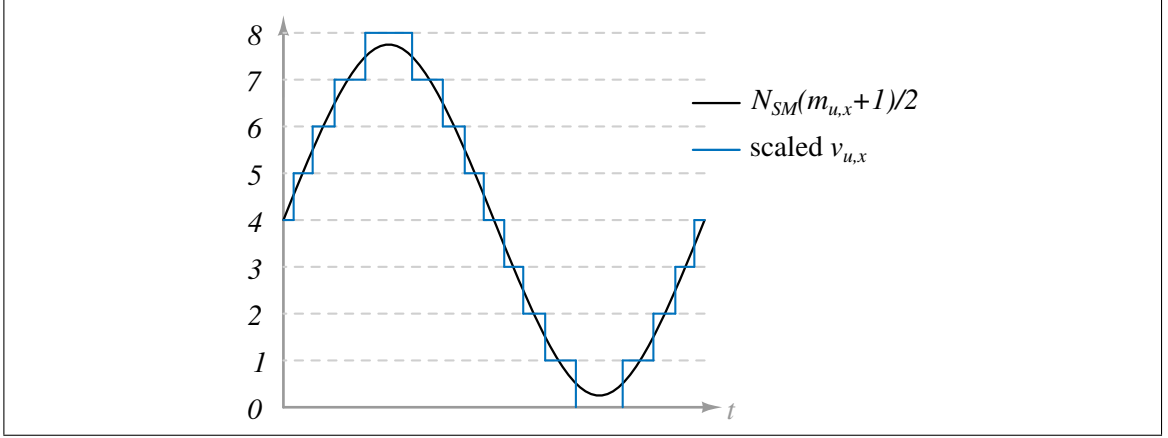


Figure 2.8. Nearest Level Control modulation concept, for $N_{SM} = 8$.

If this technique associates a particular SM with a specific level, it will generate a big unbalance in the SM capacitors, and also has inherent steady state voltage error. Thus, as said before, the modulation is complemented with sorting algorithms in order to ensure energy balance.

In this modulation, the output voltage level depends not only on the number of SMs in the stack, but also on the sampling frequency. This must be high enough to avoid a voltage step higher than one level, allowing to fully use all the available voltage levels given by N_{SM} (Tu & Xu, 2011). This will also reduce the harmonic content of the output frequency, which is always desirable.

If different sampling frequencies are used for the upper and lower arms, or if the sampling are shifted with respect to each other, the switching instants will be different for the upper and lower stacks, allowing to double the number of levels at the output voltage

(Sharifabadi, Harnefors, Nee, Norrga, & Teodorescu, 2016c). This effect is similar to the case of the PS-PWM with the displacement angle between upper and lower carriers.

As this modulation does not have a carriers to switch the devices, the harmonic spectrum is not concentrated around a specific frequency (Tu & Xu, 2011). It contains approximately all the harmonic orders, which can be reduced by increasing the number of SMs. However, increasing the number of SMs requires a higher sampling frequency in order to use all the levels. Finally, like in the LS-PWM, this modulation method also requires a sorting algorithm for balancing the SMs capacitors.

2.4. Control Structure

The MMC has a relatively complex internal dynamics due to all the passive components that compose it. For the same reason, its control is challenging and involves multiple objectives. As in every converter, the output current as well as DC-link related variables must be in the control scheme. However, due to the presence of capacitors in the SMs, the MMC requires control loops and algorithms for controlling internal variables such as the SMs voltage, arms and leg energy and the circulating currents. These variables are not directly related to the input or output variables of the converter, but they have a high impact on its performance. Controlling these variables ensures a reliably, stable and efficient operation, and thus their controls must be properly designed. Classical methods such as independent PI controllers, or more advanced methods such as predictive control can be used for this purpose (Perez et al., 2015; Debnath, Qin, Bahrani, Saeedifard, & Barbosa, 2015), but all of them have the same main objectives and considerations.

Figure 2.9 shows the general structure of a MMC control system. The high-level and output current controls are common in every converter and depends on the application and its context. Here, output power, torque or DC-link voltage references can be used for the subsequent controls. On the other hand, the arm energy and SM balancing controls are related to the internal variables of the MMC. The SMs voltage difference between the

upper and lower arms generates the circulating current, which affects the efficiency of the converter but also helps reducing the voltage ripple. The SM balancing algorithms are used to control the arms voltages and the SMs voltages inside a stack, and they define which gate signals will be triggered given the previous computations.

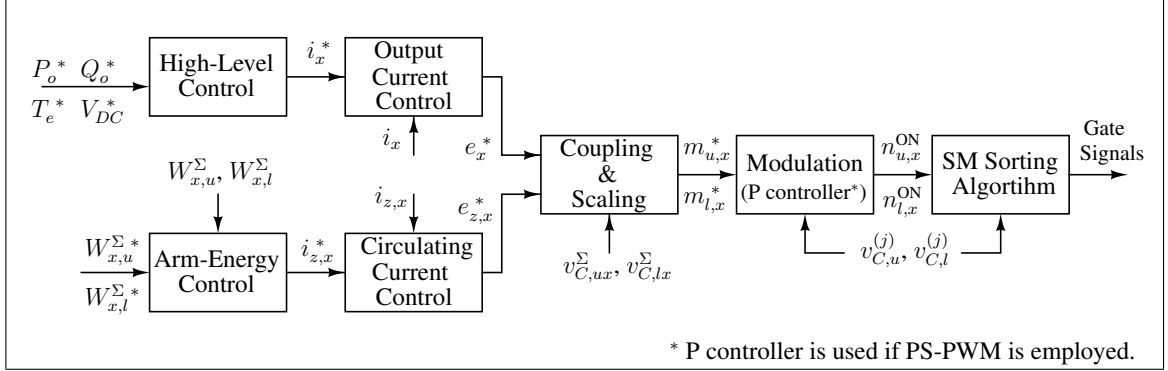


Figure 2.9. MMC general control scheme.

The output current control can be considered the most fundamental one of any converter, and must be designed with proper care in order to ensure stability and high performance. As a common and reliably method, the Proportional-Integral-Derivative (PID) controller can be used for this variable, where the derivative part is actually not considered (Isaksson & Graebe, 1999). It is easy to tune given a model, but its performance is the best for tracking DC references. If used directly for tracking AC references, no good results can be expected given its nature. Thus, for power converters the Park transformation (Park, 1929) is used in order to obtain a DC representation of the model, and then the PI controller can be used directly in this new DC system. This is nowadays a common method for controlling three-phase systems. Obviously, there are several other methods for controlling the output current. These methods include a Proportional-Resonant (PR) controller, which can track directly AC references; dead-beat control for reaching the reference with the smaller number of steps; predictive control for considering different constraints and optimize multiple variable simultaneously, etc.

The arms energy control is related to the internal dynamics of the MMC. The main objective is to balance the total energy of the upper and lower SMs stacks ($W_{x,u}^{\Sigma}$ and $W_{x,l}^{\Sigma}$) to the reference value, ensuring that it makes converge the voltage sum of the SM capacitors to the DC-link voltage V_{DC} in each stack. If the stacks energy are not controlled, undesired effects can occur given the power handled by the passive components of the legs and the overall performance is affected. Different methods consider different variables to perform this control, but it is common to use the energy as the variable to be controlled, since it eases the design of the controller.

The output of the arm energy controller is the reference for the circulating current value. As said before, the circulating current does not affect directly the output variables, but rather the internal dynamics of the converter. It actually generates a natural balancing of the capacitors even when it affects the efficiency. Thus, injecting specific harmonics on the circulating current helps balancing the stacks energy and maintain a stable operation (Pou et al., 2015), for which the arm energy control is needed. However, there are cases where the AC term of the circulating current is suppressed in order to reduce the stress on the devices and increase the efficiency. In this scenario, the reference value for the circulating current AC term is zero, and there may be no need for using the arm energy controller. The same control methods mentioned for the output current can be used for the circulating current, such as the PI control with Park transformation, resonant controller, or more advanced methods such as dead-beat or predictive control.

The output and circulating current controllers give the inner and mean EMF voltages e_x and $e_{z,x}$ to be used in the stacks. A coupling stage is made where both reference voltages are used to obtain the separated references for the upper and lower stacks. Then, the upper and lower reference voltages are scaled in order to obtain the modulating signals $m_{u,x}$ and $m_{l,x}$. There are different methods for scaling the arm voltage references (Sharifabadi, Harnefors, Nee, Norrga, & Teodorescu, 2016a). The simplest method consist of using directly the value of $\frac{V_{DC}}{2}$ to divide the arm voltage references and obtain the arm modulation signals, but this does not consider the real value of the stacks capacitors

sum. A close loop method uses the measured voltages sums of each stack to divide their respective voltage references, while an open loop method uses the reference voltage sum for each. Also, an hybrid control uses a band-pass filter to obtain the ripple components of the voltage sum, so then the DC-link value is added. Each method have their advantages, but share the same objective.

In the modulation stage the number of SMs to be active in each stack is determined. Some of the common modulation methods were briefly detailed previously in this section, where the PS-PWM is more considered among them given its equal power distribution and waveform quality. If PS-PWM is used, then a P controller can be added in this stage to increase the performance. In this method, each SM has its own modulating signal and an offset is added to it depending on the actual voltage of the respective SM. This helps balancing the the respective SMs and even increase the waveform quality.

Finally, the SM balancing algorithm is the last stage on the control. One of the simplest algorithms is the SM sorting. This simply consist on choosing which capacitor must be turned on depending on the direction of the arm current. If the current is positive through the arm, the SMs with the lowest voltages must be turned on (limited by the number of needed active SMs) so they can be charged. The SMs with higher voltages are bypassed so they do not charge even more. The same logic is considered for negative arm currents. More complex methods consider predictive sorting, where an estimation of the SMs voltages is performed.

Some methods do actually come off of the PWM modulation schemes, called tolerance band methods (Hassanpoor, Ilves, Norrga, Ängquist, & Nee, 2013). In these, the switching instant of the SMs occurs when their respective voltage crosses the upper or lower limit (which is the reason it does not consider a carrier-based scheme). The switching frequency will be higher at transients and disturbances, but is reduced at steady state, so they are efficient with respect to the dynamics of the converter. A direct consequence is that the switching frequency will vary with a non-characteristic spectrum, hindering the filter design and standard compliance.

In summary, the control structure of the MMC can be divided into two parts: the first is the external application-related controls, which includes the output current control and high-level controls such as the DC-link or AC voltages. These are directly related to the input and output variables of the converter and the desired application objective. The second is related to the internal dynamics of the converter. They are not related to the application itself, but to ensure stability on the converter. Controlling the SMs voltage and their sum, together with the circulating current, will ensure a stable, reliable and efficient operation, so the maximum performance can be obtained and the other variables can be properly controlled. Therefore, the control complexity of the MMC is higher compared to other converters, involving a lot of design, measurements, algorithms and considerations.

3. DUAL ACTIVE BRIDGE CONVERTER

3.1. Topology and operation

Figure 3.1(a) illustrates the DAB topology and its relevant variables. It consists of two H-Bridges connected to the primary and secondary side of a transformer. The transformer is usually designed to operate in the mid and high frequency range in order to minimize its size. The total series inductance L_s (transformer leakage inductance plus external inductor, if exists) serves as the instantaneous energy storage element. Depending on the direction of the power flow, one H-Bridge acts as the inverting stage while the other acts as the rectifier stage, imposing the respective input and reflected output voltages on the terminals of the inductance L_s . Assuming ideal semiconductors and transformer, the DAB can be simplified and modeled as shown in Figure 3.1(b).

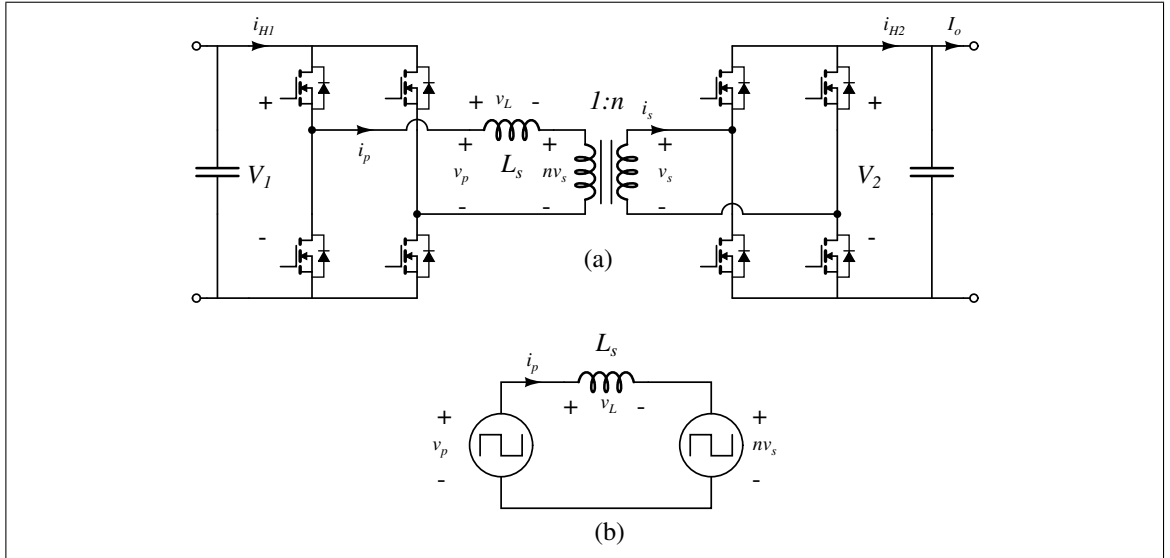


Figure 3.1. (a) Dual Active Bridge topology and (b) simplified and equivalent circuit.

The simplest modulation for the converter is named Single Phase Shift (SPS) modulation, which is illustrated in Figure 3.2. It consists of two square waves that control the primary and the secondary Full-Bridges, and the phase-shift between them

is manipulated in order to regulate the output voltage or the transferred power (Mi et al., 2008; Gorji et al., 2019). More complex modulations exists for this converter in order to increase the performance or achieve different objectives, such as Dual or Triple Phase Shift modulation (Calderon et al., 2018; Song et al., 2019), but will not be detailed in this work.

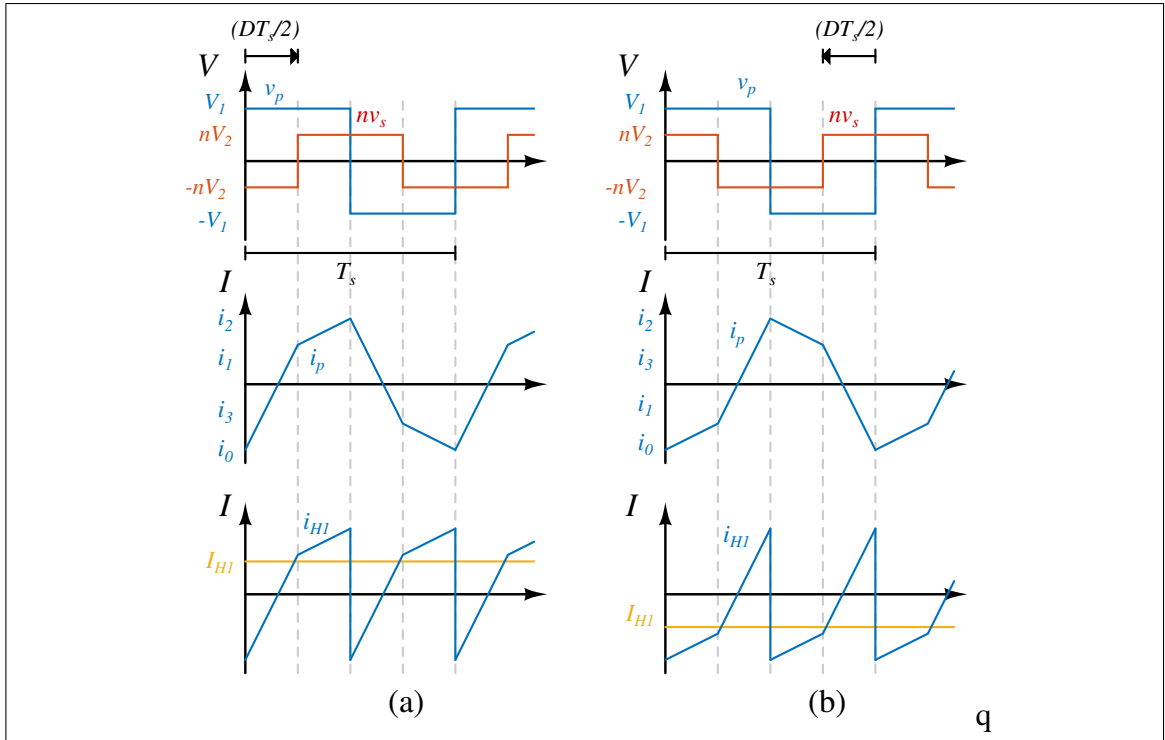


Figure 3.2. Single Phase Shift Modulation: (a) $D > 0$ and (b) $D < 0$.

3.2. Power transfer with SPS

To determine the transferred power, Figure 3.2(a) is taken as reference. T_s is the switching period, equivalent to $\frac{1}{f_s}$ with f_s the switching frequency. $D \in \{-1, 1\}$ is the variable that represents the phase shift between the square waves. $|D| = 1$ means a phase shift of 180° (or a time shift of $\frac{T_s}{2}$), and $D = 0$ means no phase shift. When $D > 0$, the primary square wave leads the secondary one and vice versa. V_1 and V_2 are the

voltages at the DC side of the primary and secondary Full-Bridges, respectively, and n is the transformer turn ratio, defined as $n = \frac{v_p}{v_s}$.

When the system is in steady state, the transformer primary side current i_p satisfies the following conditions:

$$i_0 = -i_2 \quad i_1 = -i_3 \quad (3.1)$$

where i_0 , i_1 , i_2 and i_3 are the waveform vertices of the primary side current i_p in steady state. Also, due to the waveform symmetry, only half switching cycle is needed to determine the transferred power, so the interval from $t = 0$ to $t = \frac{T_s}{2}$ is taken into account. Considering the voltages applied to the inductor L_s and eq. (3.1), the following equations are obtained:

$$i_1 = i_0 + \frac{(V_1 + nV_2)}{L_s} \frac{DT_s}{2} \quad -i_0 = i_1 + \frac{(V_1 - nV_2)}{L_s} \frac{(1 - D)T_s}{2} \quad (3.2)$$

Solving eq. (3.2) for i_0 and i_1 , they can be expressed in terms of other variables:

$$i_0 = (nV_2 - V_1 - 2DnV_2) \frac{T_s}{4L_s} \quad i_1 = (nV_2 - V_1 + 2DV_1) \frac{T_s}{4L_s} \quad (3.3)$$

The average power in the DC input is calculated to obtain the transferred power during the first half-cycle:

$$P_{DAB} = \frac{2}{T_s} \int_0^{\frac{T_s}{2}} V_1 i_p(t) dt = \frac{2V_1}{T_s} \int_0^{\frac{T_s}{2}} i_p(t) dt \quad (3.4)$$

From eq. (3.4), the average value of the current i_p in the first half-cycle must be determined. Using the relations obtained in eq. (3.3), replacing them in eq. (3.4) and solving the integral, the power transferred with SPS modulation is given by:

$$P_{DAB} = \frac{nV_1V_2}{2f_sL_s} D(1 - |D|) \quad (3.5)$$

Thus, the transferred power depends on the input and output voltages, the turn ratio, the total series inductance L_s , the switching frequency f_s , and the phase-shift D . The absolute value is used in order to represent the positive or negative power transfer, depending on the sign of the phase-shift D . The maximum power transfer occurs when $|D| = 0.5$, shown in eq. (3.6), and values greater than this do decrease the transferred power.

$$P_{DAB,max} = \frac{nV_1V_2}{8f_sL_s} \quad (3.6)$$

Figure 3.3 shows the normalized power as function of the phase-shift D . In SPS, since the maximum power is produced when $|D| = 0.5$, only the range $-0.5 \leq D \leq 0.5$ is considered.

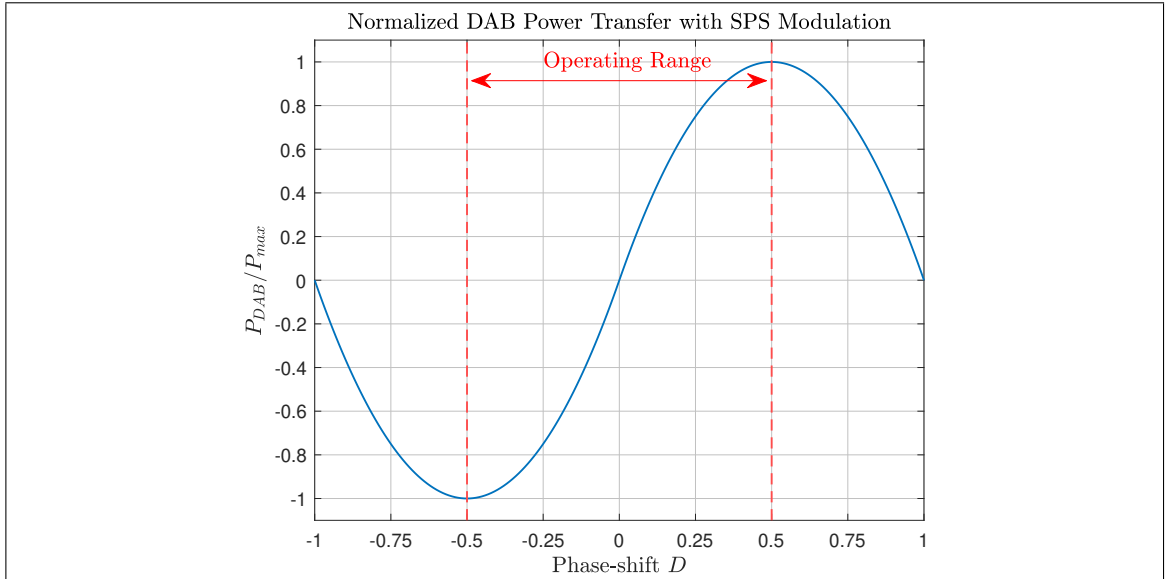


Figure 3.3. DAB normalized power transfer.

3.3. Zero Voltage Switching (ZVS)

ZVS refers to the condition where a transistor is turned on with zero or a really low voltage on its conducting terminals. In this way, there is no loss in the turning on process of the transistor, since the power, the product of the current and voltage, is zero or close

to zero. This condition is particularly beneficial for high frequency applications, where the reduction of the switching losses can greatly increase the efficiency of the converter (Shao et al., 2019). In order to achieve ZVS, the energy stored in the transistor parasitic capacitance must be discharged, which depends on the direction and the amount of current that was being handled. Although the parasitic capacitance is not totally discharged, losses are still partially reduced.

For the DAB, the conditions for ZVS on each of the H-Bridges depend on the transformer current i_p at the switching transitions (see Figure 3.1 and 3.2).

$$\underbrace{i_0 < 0}_{\text{For primary H-Bridge}} \quad \underbrace{i_1 < 0}_{\text{For secondary H-Bridge}} \quad (3.7)$$

If both conditions in (3.7) are met (and assuming enough current), fully ZVS is achieved in the converter. However, it may be the case where only one of the conditions is met and only one H-Bridge operates in ZVS condition. Replacing eq. (3.3) into (3.7), the conditions for ZVS can be expressed as follows:

$$\underbrace{\frac{(M-1)}{2M} < D}_{\text{For primary H-Bridge } H_1} \quad \underbrace{\frac{(1-M)}{2} < D}_{\text{For secondary H-Bridge } H_2} \quad (3.8)$$

Here, M denotes the reflected voltage ratio between the DAB input and output voltages (not to be confused with the transformer turn ratio n):

$$M = \frac{nV_2}{V_1} \quad (3.9)$$

From eq. (3.8), the ZVS of each H-Bridge depends on the phase-shift D and the input and output voltage. These conditions are plotted in Figure 3.4 in order to have a better understanding of the converter ZVS operation. H_1 and H_2 refers to the primary and secondary H-Bridges, respectively.

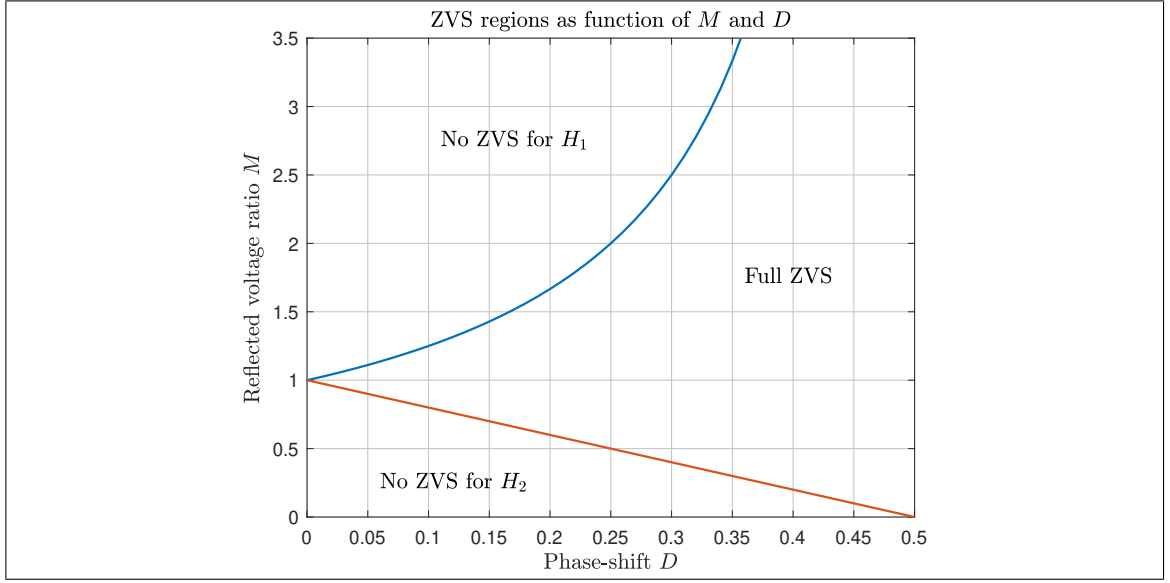


Figure 3.4. Dual Active Bridge ZVS regions.

As can be inferred from the plot, the higher the value of the phase-shift D , the higher the range of full ZVS for $M \neq 1$. When $M = 1$, the converter always operates in full ZVS condition independently of the phase-shift D . This is the reason the DAB is mostly used for fixed input and output voltage applications. It is designed to work with fixed M , but with an operating range for D that ensures full ZVS at the different power transfer it must withstand.

The previous analysis is for the ideal ZVS region. It does not consider other effects such as the dead-time, transistors capacitance discharge or the transformer parasitic components and magnetic behavior, which slightly modify the curve on Figure 3.4 (Shao et al., 2019). However, it gives a good enough start point to design the converter.

4. ARM LINK ENHANCED MODULAR MULTILEVEL CONVERTER

All the benefits of the Modular Multilevel Converter make it ideal for high and medium voltage ranges, where HVDC is one of the most considered applications. It was seen that the structure and operation of the MMC requires large capacitance in the SMs and dedicated control algorithms in order to minimize the voltage ripple. This increases the converter volume and its control complexity, specially when a high number of SMs are used, which can easily reach more than a hundred of SMs per stack in the high voltage range. Industry and academia have deeply studied and addressed these issues, and even nowadays new methods or strategies are constantly being proposed. However, most of these solutions are focused for the high and medium voltage range, and the low voltage range is barely considered. Due to the large SMs capacitance, numerous sensors and electrical connections, it is not very suitable for lower power and voltage applications, since the cost, complexity and required space does not compare against other available solutions (Ashourloo et al., 2018).

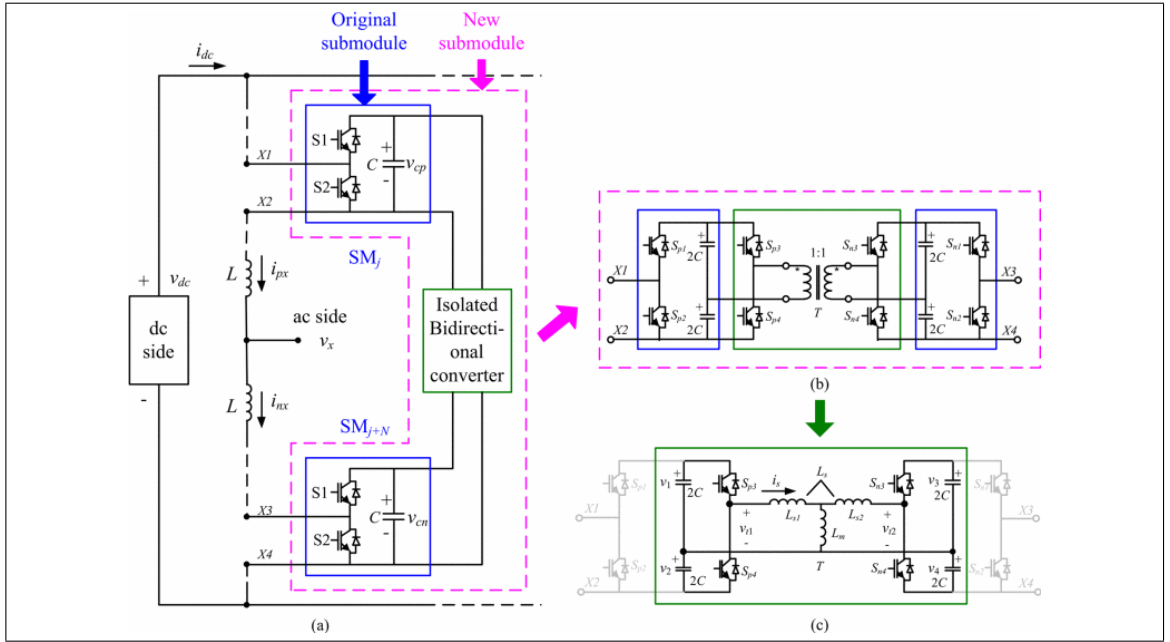


Figure 4.1. MMC topology proposed by (He et al., 2015).

Few works have considered strategies to extend the MMC to low voltage applications, and extra circuit addition is not very considered in order to improve some aspects. A new MMC with power channels between upper and lower SMs was proposed for medium voltage drive, using a simple DC-DC converter (He et al., 2015). Its topology is shown in Figure 4.1. As can be seen, a Dual Half-Bridge topology is used to transfer the power between channels, where the SMs midpoint voltage is required. This allows to reduce the capacitance and operate at low frequencies, focusing in medium voltage applications. However, its control still involves voltage measurement circuitry and more control requirements.

Another new MMC topology uses a three-port transformer to cancel the voltage ripple via magnetic flux cancellation, so electrolytic capacitors are not needed (Irfan et al., 2021). The topology is illustrated in Figure 4.2. It connects each SMs with the corresponding one from the other legs, and the SMs capacitors are connected to the three-port transformer with a Half-Bridge, needing the SMs voltage midpoint. Taking advantage the power ripple phase of each leg, it is transferred by each SM to the transformer and is canceled via magnetic flux addition. Still this method also involves voltage measurements and is intended for high voltage applications. Additionally, the circuitry needed is relatively complex to implement in the converter.

The converter analyzed on this work is named Arm-Link Enhanced MMC (ALE-MMC), which allows to extend the MMC to low-voltage and variable frequency applications (Tarisciotti, Costabeber, Tardelli, & Cardenas, 2019). Its basic principle is to transfer the power ripple of an upper SM to a lower one (and vice versa) by employing a Dual Active Bridge converter. Considering the PS-PWM, all the SMs of a stack have virtually the same behavior, thus their voltage ripple are equal. Also, the upper and lower stacks have voltage oscillations that behave opposite to an extent. This means, when an upper SM capacitor is being charged, a lower one is discharged. The ALE-MMC takes advantage of these properties and uses the DAB to transfer the excess of charge from one

capacitor to another, greatly reducing the ripple in the DC-side of the SMs, even at low frequencies, including zero-frequency output.

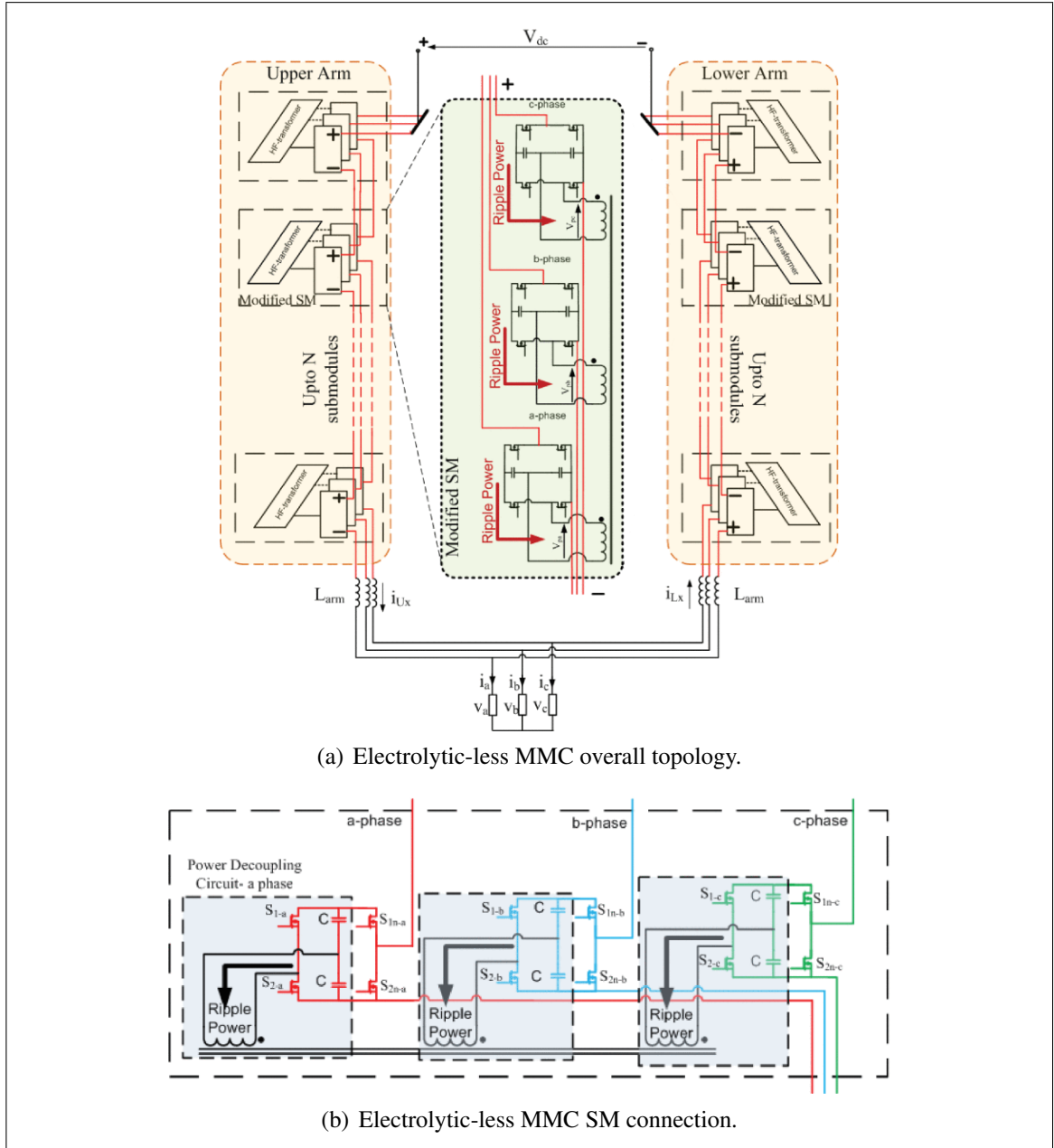


Figure 4.2. MMC topology proposed by (Irfan et al., 2021).

This chapter will describe the topology and the mathematical analysis of the ALE-MMC, including how to operate it and the considerations that must be taken when

designing the converter. In a brief summary, the MMC part of the converter can be operated normally but with simplified complexity, while the DAB can be operated in an open loop control, requiring only current measurements and no voltage measurements.

4.1. Topology

The ALE-MMMC maintains the MMC basic structure with the series-connected SMs. The main modification is that DABs are used to inter-link each of the upper SMs of a leg with the lower ones, allowing the power transfer between them. Figure 4.3 shows a single-phase or leg of the ALE-MMC topology, while Figure 4.4 shows its sub-circuits.

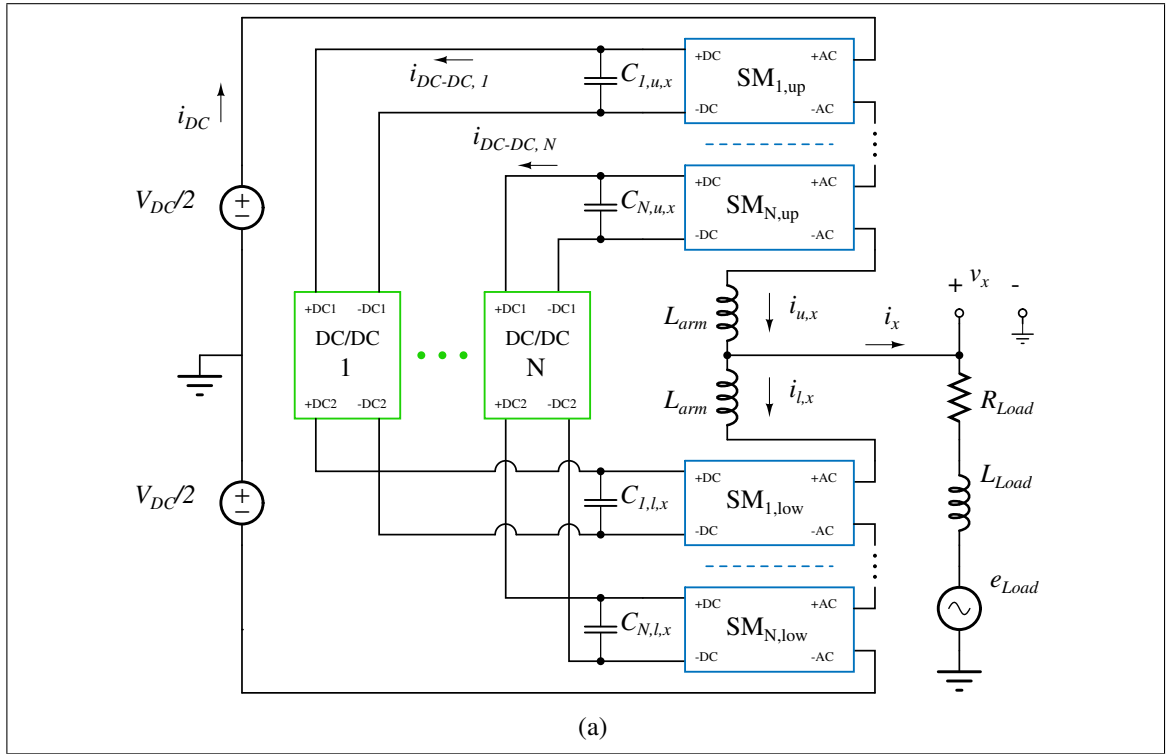


Figure 4.3. Single leg Arm-Link Enhanced MMC topology.

As can be seen, the first SM of the upper stack is linked to the first of the lower one and so on. For a converter with N_{SM} SMs per stack, then the same number of DABs are needed per leg, and their transformer turn ratio is 1:1. Due to the incorporation of the DAB, it can

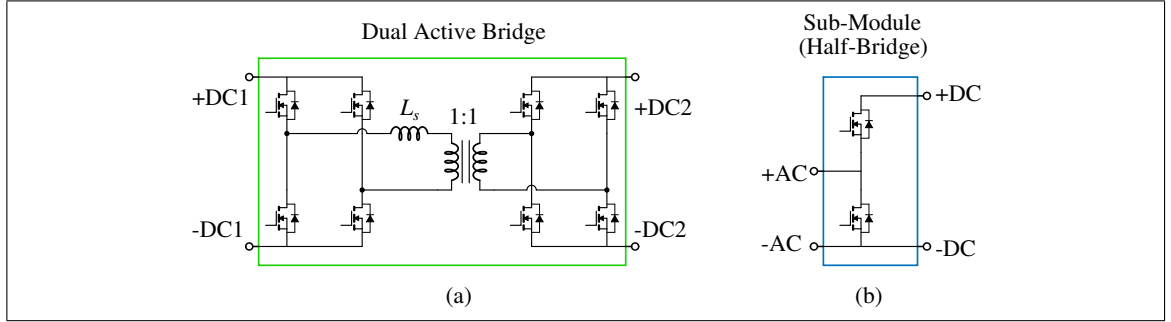


Figure 4.4. ALE-MMC sub-circuits: (a) Dual Active Bridge and (b) Half-Bridge.

be considered that each SM needs four additional semi-conductor devices. This means an increase of 200 % in the number of transistors needed for the converter, plus the addition of N_{SM} transformer per phase.

The reasons of choosing the DAB for the power transferring are all the benefits it provides. It allows the use of high-frequency transformer so the volume is reduced, and also has the advantage of zero-voltage switching (ZVS). But most importantly, it provides galvanic isolation which is required for the operation. Recalling Figure 3.4, when the input and reflected output voltage are equal there is always ZVS in both H-Bridges. In the ALE-MMC case, the transformer ratio is 1:1 and both DC voltages of the H-Bridges are (in average) the same. Thus, the DAB will operate always in the full ZVS zone. On the other hand, using SPS modulation the control of the DAB is relatively simple, and no complex control algorithms are added, as the next section will describe.

4.2. Operation

Regarding the control of the MMC-side of the studied converter, no major changes are made with respect to the original topology. It is important to recall that the PS-PWM is chosen to operate the converter, since this produces equal power stress on all the SMs of an stack. Regarding the displacement angle θ_d , it is chosen so that it eliminates the switching harmonics in the circulating currents for reasons that will be clarified later in this chapter, resulting in $N_{SM} + 1$ levels on the output voltage. Therefore, a single carrier

is used for each of the coupled upper and lower SMs if N_{SM} is even. All the equations seen in Chapter 2 can be used in the ALE-MMC, so the decoupled models and the modulated voltages apply for this part.

Recalling equation (2.1), the voltages modulated by each arm stack are:

$$\begin{aligned} v_{u,x} &= \frac{V_{DC}}{2} + m_{u,x} \frac{V_{DC}}{2} \\ v_{l,x} &= \frac{V_{DC}}{2} + m_{l,x} \frac{V_{DC}}{2} \end{aligned} \quad (4.1)$$

where $v_{u,x}$ and $v_{l,x}$ are the modulated voltages of the upper and lower arm stacks, respectively, while $m_{u,x}$ and $m_{l,x}$ their modulating signals, respectively.

It is also useful to recall the transformation matrix for the decoupled variables:

$$\begin{bmatrix} i_x \\ i_{z,x} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{u,x} \\ i_{l,x} \end{bmatrix} \quad (4.2)$$

$$\begin{bmatrix} e_x \\ e_{z,x} \end{bmatrix} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{u,x} \\ v_{l,x} \end{bmatrix} \quad (4.3)$$

As stated in the previous chapters, e_x is the inner emf that drives the output current i_x , and $e_{z,x}$ is the mean voltage between the upper and lower arm which can control the circulating current $i_{z,x}$. In this sense, the modulating signals of the arms can be separated in two terms:

$$\begin{aligned} m_{u,x} &= -m_x - m_{z,x} \\ m_{l,x} &= m_x - m_{z,x} \end{aligned} \quad (4.4)$$

where m_x is the modulating signal for the output or inner leg voltage, while $m_{z,x}$ is the modulating signal for the mean arm voltage. Using equations (4.1), (4.3) and (4.4) the following is obtained:

$$\begin{aligned} e_x &= \frac{V_{DC}}{2} m_x \\ e_{z,x} &= \frac{V_{DC}}{2} - \frac{V_{DC}}{2} m_{z,x} \end{aligned} \quad (4.5)$$

In order to control the output and circulating current, the output of the controllers must give the values for m_x and $m_{z,x}$, which should be sinusoidal in normal operation. So, the primary and basic control of the currents does not differ from the original topology, and the same techniques and methods can be used for them.

The main difference comes on how the balancing of the SMs voltages is performed. In the classical MMC, both arms energy and SMs voltages are balanced with dedicated control loops and sorting algorithms based on voltage measurements. However, considering the low voltage range, the ALE-MMC avoids the voltage measurements in order to simplify the system control. As said previously, this is achieved by relying on the upper and lower SMs voltage symmetry given by the PS-PWM.

The DAB is used to transfer the excess of charge from one capacitor to another, with the main objective of reduce the voltage ripple on the SMs terminals. For this to work, it is necessary to determine the current needed to transfer the excess of charge. In order to ease the understanding of the DAB operation in the ALE-MMC, the DAB is replaced with an ideal DC-DC transformer with 1:1 turn ratio, and only 1 SM per stack is considered. The operating principle can be easily extended to the N_{SM} SMs case. Figure 4.5 shows the idealized and simplified model.

i_{DC-DC} is the current handled by the ideal DC-DC transformer, while s_u and $s_l \in \{-1,1\}$ are the upper and lower switching signals, respectively, where 1 means the ON state and -1 the OFF state. $v_{C,u}$ and $v_{C,l}$ are the voltages of the upper and lower SM capacitors, respectively, and C their capacitance. Considering the PS-PWM, there are four possible states depending on the semiconductor switching signals:

$$s_u \text{ and } s_l \text{ OFF: } \begin{cases} -C \frac{d}{dt} v_{C,u} = i_{DC-DC} \\ C \frac{d}{dt} v_{C,l} = i_{DC-DC} \end{cases} \quad (4.6)$$

$$s_u \text{ ON and } s_l \text{ OFF: } \begin{cases} i_{u,x} - C \frac{d}{dt} v_{C,u} = i_{DC-DC} \\ C \frac{d}{dt} v_{C,l} = i_{DC-DC} \end{cases} \quad (4.7)$$

$$s_u \text{ OFF and } s_l \text{ ON: } \begin{cases} -C \frac{d}{dt} v_{C,u} = i_{DC-DC} \\ -i_{l,x} + C \frac{d}{dt} v_{C,l} = i_{DC-DC} \end{cases} \quad (4.8)$$

$$s_u \text{ and } s_l \text{ ON: } \begin{cases} i_{u,x} - C \frac{d}{dt} v_{C,u} = i_{DC-DC} \\ -i_{l,x} + C \frac{d}{dt} v_{C,l} = i_{DC-DC} \end{cases} \quad (4.9)$$

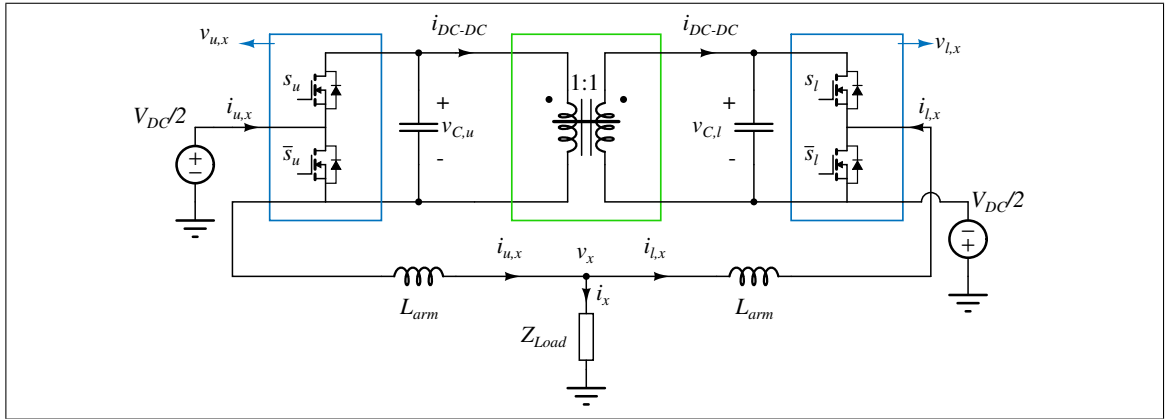


Figure 4.5. Simplified model with ideal DC-DC transformer and 1 SM per stack.

Considering the transformer turn ratio $n = 1$ as shown in Figure 4.5, from equations (4.6) to (4.9), the switched model can be written as follows:

$$\begin{aligned} i_{DC-DC} &= \frac{(s_u + 1)}{2} i_{u,x} - C \frac{d}{dt} v_{C,u} \\ i_{DC-DC} &= -\frac{(s_l + 1)}{2} i_{l,x} + C \frac{d}{dt} v_{C,l} \end{aligned} \quad (4.10)$$

Averaging the model over one fundamental cycle, the current i_{DC-DC} that the DC-DC transformer must handle can be obtained in terms of the modulating signals and the arm currents:

$$i_{DC-DC} = \frac{1}{4} [(i_{u,x} - i_{l,x}) + m_{u,x}i_{u,x} - m_{l,x}i_{l,x}] + \underbrace{\frac{C}{2} \frac{d}{dt}(v_{C,l} - v_{C,u})}_{= 0 \text{ since } v_{C,l} \approx v_{C,u} \text{ is assumed}} \quad (4.11)$$

The above equation represents the current needed to maintain the capacitors with low voltage ripple. It is assumed that $v_{C,u} \approx v_{C,l} = v_C$ due to the ideal DC-DC transformer, where v_C is the nominal voltage of the SM capacitor. Therefore, the last term the equation is null. Two things are relevant from equation (4.11). The first, is that the reference current that the DC-DC transformer must handle does not depend on the SM voltages given the assumption. Second, it depends on the arm modulating signals and the arms currents, so it is clear that it will have an AC behavior with different harmonic content, which will be discussed later. All the variables needed are known from control computation and from measurements, so the DC-DC current can easily be calculated.

With this current determined, the final step is to determine how the DAB will handle this current in the real converter. For this, equation (3.5) is recalled, which determines the power handled by the DAB:

$$P_{DAB} = \frac{nV_1V_2}{2f_sL_s}D(1 - |D|) \quad (4.12)$$

Where V_1 and V_2 are the voltages at the DC-side of the input and output, respectively, n the transformer turn ratio, L_s the equivalent series inductance, f_s the DAB switching frequency and D the normalized phase-shift. In this case of study, $n = 1$ and $V_1 \approx V_2 \approx v_C$. Hence, the instantaneous power the DAB must handle is $p_{DAB} = i_{DC-DC}v_C$, where both variables are known. Knowing this power and replacing this value in (4.12), the equation is solved to obtain the phase-shift D needed to transfer the current i_{DC-DC} :

$$D = \frac{1}{2} \left[1 - \sqrt{1 - \frac{|p_{DAB}|}{P_{max}}} \right] \text{sign}(i_{DC-DC}) \quad (4.13)$$

where P_{max} is the maximum power transfer given by (3.6), which in this case is

$$P_{max} = \frac{v_c^2}{8f_s L_s} \quad (4.14)$$

In summary, in order to have low voltage ripple on the SM capacitors, the current in (4.11) must be transferred by the DAB, which is achieved by using the phase-shift D given in (4.13). The variables needed are the arm currents, the arm modulating signals, the DAB parameters and the nominal SM voltage v_c (which is $\frac{V_{DC}}{N_{SM}}$). In the case with N_{SM} per stack the same analysis applies and all the DABs must transfer the same current, only changing the nominal SM voltage $v_c = \frac{V_{DC}}{N_{SM}}$ for the same DC-link. Thus, the mode of operation of the DAB does not change with the number of SMs and the phase-shift D is replicated in every of them.

Another aspect of this mode of operation is that any voltage difference between both upper and lower SM capacitors is damped automatically to an extent. If current is transferred from the upper capacitor to the lower, and a sudden increase on the upper capacitor occurs, the voltage difference in the DAB transformer increases, and consequently the current transferred. In a similar way, if a decrease in the upper voltage occurs, the voltage difference in the transformer decreases, transferring less current. Thus, there exists a natural tendency to partially compensate voltage differences between the upper and lower SMs, but still the above control must be used.

An important thing to notice is that none of the instantaneous voltages of the SMs are needed (only the nominal SM voltage is required). This allows to operate the converter without voltage measurements, simplifying the control complexity and measurement systems while securing a safe voltage level on the SMs. Another highlight is that the DAB can be controlled in open loop by applying directly the obtained phase-shift D in the SPS control. This also simplifies the control complexity since no tuning is needed in order to achieve the objective.

4.3. Design considerations

As the ALE-MMC incorporates more circuitry in the converter, specific behaviors and effects must be considered regarding this addition. Moreover, as the ALE-MMC is intended for variable frequency applications, considerations about the operating frequency range must be taking into account, which some of them also apply for the classical MMC topology. Knowing these different effects will allow to guide and improve the operation of the ALE-MMC at different frequencies or scenarios.

4.3.1. Circulating Current Resonance

The amount of passive components connected in series that the MMC presents must be specially considered if the converter is intended to operate with variable fundamental frequency. As seen before, the circulating current flows through the converter leg meaning that its path comprises all the leg active SMs plus both of the arm inductors, all of them connected in series. Previous models do not show this path explicitly, and as the MMC is used in applications with fixed frequency, it is not a relevant issue.

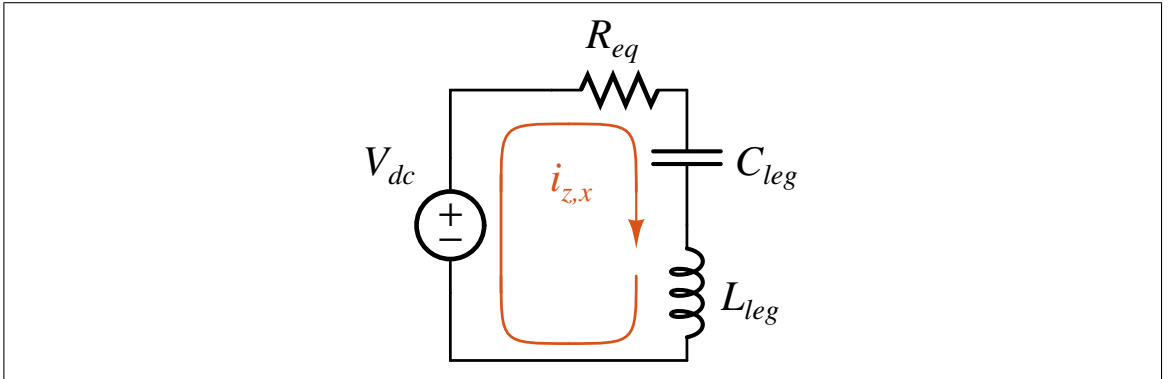


Figure 4.6. Circulating current resonant circuit.

Figure 4.6 illustrates the full path of the circulating current in the converter. C_{leg} and L_{leg} are the total series capacitance and inductance, respectively, and R_{eq} is the equivalent series resistance of the leg. Thus, the circulating current will have a resonant frequency

equivalent to:

$$f_{res,z} = \frac{1}{2\pi} \frac{1}{\sqrt{C_{leg}L_{leg}}} \quad (4.15)$$

Even if this relation is simple, the exact value of C_{leg} is uncertain. This is due to the fact that the stacks are constantly switching their SMs, changing the number of capacitors in series. Therefore, the resonant frequency varies with the time.

With PS-PWM, the average value of active capacitors on a stack is $\frac{N_{SM}}{2}$, half the number of SMs per stack. From Figure 4.5, it can be seen that the capacitance can be reflected, and hence is doubled from the perspective of the current flowing. With this, and considering the two stacks in the leg, the average value of C_{leg} can be estimated as:

$$C_{leg}^{(average)} \approx \frac{2C_{SM}}{N_{SM}} \quad (4.16)$$

where C_{SM} is the SM capacitance. In a similar way, the value of L_{leg} is constant and can be determined as:

$$L_{leg} = 2L_{arm} \quad (4.17)$$

With these equations, the average resonant frequency of the circulating current can be estimated, and it will oscillate around this value. Considering the second harmonic behavior of the circulating current, its resonance will occur when the fundamental frequency f_0 of the converter approaches half of the circulating current resonant frequency ($f_0 = \frac{f_{res,z}}{2}$).

The fact of having a resonance in the circulating current directly affects the current stress of the semi-conductor devices. When the resonance is produced, the second harmonic component of the circulating current can reach high values, and even increase the voltage ripple instead of helping reducing it. Hence, when the fundamental frequency approaches the critical value, it is recommended to suppress the circulating current second harmonic in order to reduce the conduction losses.

However, it is not recommend to suppress the circulating current in all the operation frequency range. Even if the implementation of the DAB helps reducing the SMs voltage

ripple, the circulating current also helps reducing it. This is specially crucial at low fundamental frequencies, where the voltage ripple is higher due to the longer time the SMs are active. Based on this, the suppression of the circulating current should be made at higher frequencies and when the resonance value is being reached. Ideally, the resonant frequency should be far from the low frequency range if possible.

4.3.2. DAB Frequency Response

In order to transfer the power ripple between capacitors, a Dual Active Bridge is employed. This converter is designed for DC-DC power transfer, but this application uses it to transfer AC power. It maintains a mean DC voltage on its input and output terminals, but the current transferred (or its phase-shift) has an AC behavior with different harmonic content. Given this, it is important to consider the frequency response of the DAB.

It has been demonstrated that the DAB behaves as a low-pass filter when considering control-to-output transfer functions (Qin & Kimball, 2012). This means that the effects of high frequency AC inputs will be diminished at the output. Figure 4.7 shows different control-to-output gain curves: Full-order continuous-time model proposed by Qin & Kimball (dashed line), reduced order continuous-time model (solid line) and full-order discrete-time model (dash-dot line). Results from detailed switching simulation (crosses) and results from hardware measurement (circles) are also included. All of them clearly shows that the DAB behaves as a low-pass filter.

Hence, the DAB will have a better performance at lower input frequencies. When the input D is AC instead of DC, it adds currents of the same input frequency in the high-frequency transformer, which is designed to operate at much higher frequencies (e.g. 50 kHz). The transformer will have to withstand these additional currents (~ 0 to 2 kHz, depending on the fundamental frequency range), together with the currents of its nominal operation frequency.

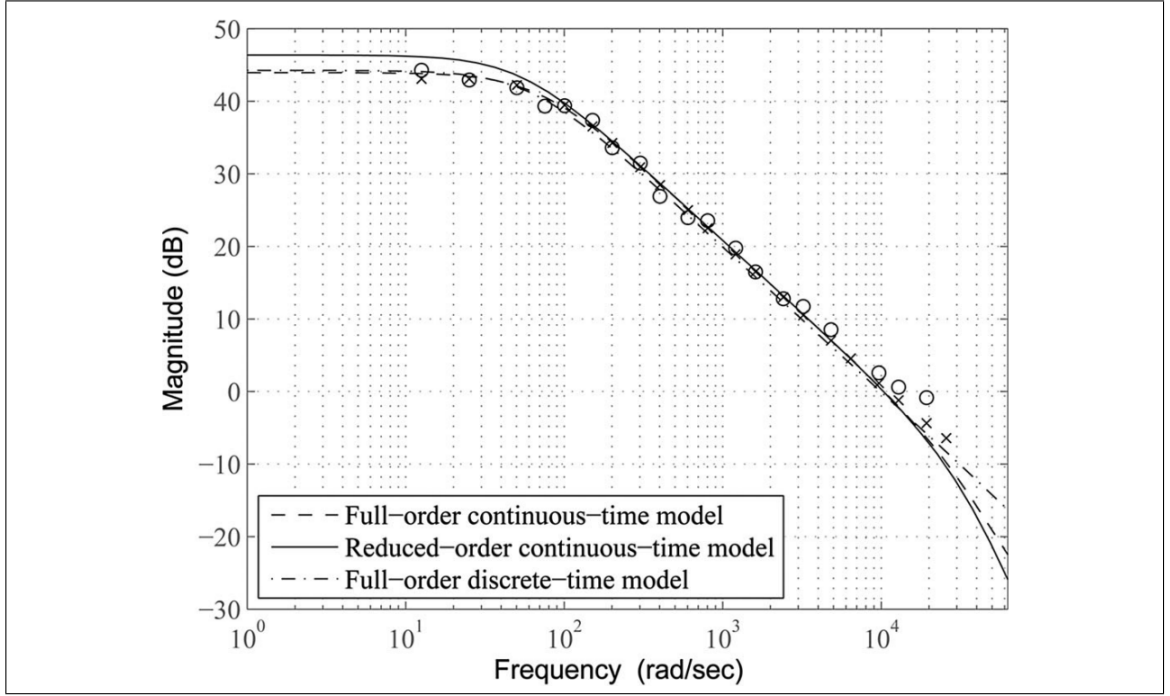


Figure 4.7. Dual Active Bridge control-to-output gains curves for different models and experiments (Qin & Kimball, 2012).

A lower performance on the DAB translates on more core losses, and in this particular application it also means a higher voltage ripple on the SMs capacitors. Considering this, it is desirable to reduce the harmonic content in the DABs transformer in order to increase the performance, since the ALE-MMC operates at variable frequency.

4.3.3. DAB Current Harmonic Content

Given the frequency response of the DAB, it is of interest to determine the harmonic content it will handle in normal operation of the ALE-MMC. Considering that the DAB current depends on the arm currents and their modulating signals, it can be expressed in terms of the output and circulating current related variables. Using the transformation matrix in (4.2) and equation (4.4), the DC-DC current in equation (4.11) can be expressed as:

$$i_{DC-DC} = \frac{i_x}{4} - \frac{i_x m_{z,x}}{4} - \frac{i_{z,x} m_x}{2} \quad (4.18)$$

The output current is expressed as:

$$i_x = I_o \sin(\omega_0 t - \varphi_L) \quad (4.19)$$

with φ_L the load angle. The phase angle ϕ_x is omitted for ease of understand. In this analysis, it is assumed that the circulating current has the DC component plus a second-harmonic current, while higher harmonics are neglected. Hence, equation (2.23) is simplified to:

$$i_{z,x} = \frac{I_{DC}}{3} + I_{2,z} \sin(2\omega_0 t + \phi_{2,zx}) \quad (4.20)$$

where I_{DC} can be expressed in terms of the peak output current I_o with equation (2.19).

On the other hand, the inner or output emf m_x and the mean arm voltage $m_{z,x}$ modulating signals can be expressed as follows:

$$\begin{aligned} m_x &= \hat{m}_o \sin(\omega_0 t) \\ m_{z,x} &= \hat{m}_z \sin(2\omega_0 t + \phi_{mz,x}) \end{aligned} \quad (4.21)$$

where $\hat{m}_o$ and $\hat{m}_z$ are the output and mean voltage modulating signals amplitude, respectively, and $\varphi_{m,zx}$ is the phase-shift of the mean voltage signal. Again, the 120° shifts are omitted in m_x . It is clear that $m_{z,x}$ will have twice the fundamental frequency since only the second harmonic is considered in the the circulating current.

Finally, replacing equations (4.20) and (4.21) into (4.18), and using equation (2.19) and trigonometric identities, the DAB current can be re-written as:

$$\begin{aligned} i_{DC-DC} &= \frac{I_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{I_o \hat{m}_o^2}{8} \cos(\varphi_L) \sin(\omega_0 t) \\ &\quad - \frac{I_o \hat{m}_z}{8} [\cos(\omega_0 t + \varphi_L + \phi_{2,zx}) - \cos(3\omega_0 t - \varphi_L + \phi_{2,zx})] \\ &\quad - \frac{I_{z,2} \hat{m}_o}{4} [\cos(\omega_0 t + \phi_{2,zx}) - \cos(3\omega_0 t + \phi_{2,zx})] \end{aligned} \quad (4.22)$$

From equation (4.22), it is clear that the current handled by the DAB will have both fundamental frequency and third-harmonic components. If there is no circulating current

control, then $\hat{m}_z = 0$ and the third harmonic amplitude will be determined mainly by the circulating current second harmonic amplitude, $I_{z,2}$, for a given $\hat{m}_o$.

As seen previously, to the DAB transformer nominal current will be added currents with the same input signal frequencies. The higher the input frequencies, the higher the magnitude of these additional currents. Considering equation (4.22), it is expected that fundamental and third harmonic currents will be added to the DAB transformer in normal operation. Thus, at the moment of design, these additional currents must be considered in the sizing of the transformer.

4.4. Control Structure

In the classical MMC topology, the leg energy and SMs voltage balancing algorithms play a big role in the control system of the converter. In the ALE-MMC, thanks to the addition of the DABs there is no need to implement voltage or energy balancing dedicated logic. Thus, the control algorithm is greatly simplified and the computational burden is greatly reduced.

Anyway, considering the variable frequency operation of the converter, other control and operation logic must be implemented in order to achieve the best performance in each scenario. For this, the previous considerations and analysis are used as a guide for the different conditions.

Figure 4.8 shows the control structure including all the measurements needed, where i_x^* is the phase x reference output current and $i_{z,x}^*$ the phase x reference circulating current. Both output and circulating current are in a closed-loop control and any of the known control methods can be used. These control techniques can be the classical PI controller in the DQ-frame, resonant controller, model-predictive control, etc. The models and equations derived in Chapter 2 for the MMC can be used as a start point to tune the controllers.

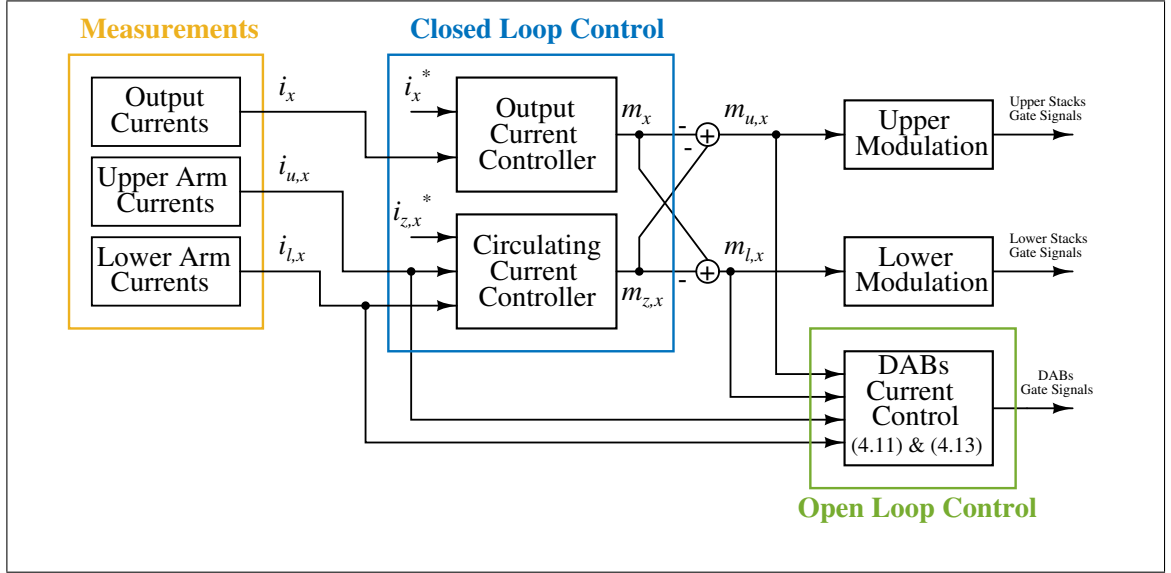


Figure 4.8. Control diagram for the ALE-MMC.

On the other hand, the DABs switching signals come from an open-loop controller, which uses only the arms currents and modulating signals to calculate the phase-shift. This calculation is based on equations (4.11) and (4.13) derived previously in this chapter. As can be seen, no voltage balancing algorithms are used, but it can be considered that the DABs actively performs this task only based on the actual current on the arms and the stacks modulation.

In order to perform all the control logic in the converter, only current measurements are needed and no voltage measurements appear on the scheme, which is an attractive feature of the topology. Thus, for a three-phase converter only nine current sensors are needed for the entire system. Considering the relation $i_x = i_{u,x} - i_{l,x}$, then the number of current sensors can be reduced to only six for the converter, but in order to have a robust system it is preferred to employ all of them.

4.4.1. Output Current Controller

The methods and techniques for controlling the output currents of a three-phase converter are commonly the same between different configurations. Methods such as

Proportional Integral (PI) controller in synchronous frame (DQ), Proportional Resonant (PR) controllers, Dead Beat Control, Model Predictive Control (MPC) and its variations, etc., can be used depending on the control main and secondary objectives.

In this work, the known synchronous PI control in the DQ-frame is used for controlling the output currents. Considering that the PI controller is not suitable for tracking AC signal references, this technique is based on transforming the three-phase AC output currents into DC quantities so the PI control can be used without problems. The Clarke-Park transformation matrix, shown in equation is used in order generate the DC equivalent variables from the AC variables. The transformation is shown in equation (4.23), where T_{dqz} is the DQZ-transformation matrix.

$$\begin{bmatrix} d \\ q \\ z_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} = T_{dqz} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (4.23)$$

Here, $\theta = \omega_0 t$ is the angle that results from the reference frequency used for the rotating reference frame, and a , b and c are the AC variables to be transformed. d and q are the DC representation of the AC quantities in a two-axis system, which are designated as the direct and quadrature variables. These designation refers to the the alignment that exist between the variables involved. For example, this version of T_{dqz} aligns the d axis with the a -phase, which will serve as the reference phasor. z is the zero component of the new two-axis DC system, and is equivalent to the common or average value of the three AC variables. In a balanced system, this z_0 component is zero, but it may have a non-zero value in some applications or operating conditions.

The model of the output current obtained in (2.8), can be re-written in its vector form for the three phases as:

$$L_{ac} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R_{ac} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} e_a - e_{Load,a} - v_{cm} \\ e_b - e_{Load,b} - v_{cm} \\ e_c - e_{Load,c} - v_{cm} \end{bmatrix} \quad (4.24)$$

where $L_{ac} = \frac{L_{arm}}{2} + L_{Load}$ and $R_{ac} = \frac{R_{arm}}{2} + R_{Load}$. Applying the DQZ-transformation matrix T_{dqz} to equation (4.24), the following is obtained:

$$L_{ac} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_{z0} \end{bmatrix} + \begin{bmatrix} R_{ac} & -\omega_0 L_{ac} & 0 \\ \omega_0 L_{ac} & R_{ac} & 0 \\ 0 & 0 & R_{ac} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_{z0} \end{bmatrix} = \begin{bmatrix} e_d - e_{Load,d} \\ e_q - e_{Load,q} \\ e_{z0} - e_{Load,z0} - v_{cm} \end{bmatrix} \quad (4.25)$$

Equation (4.25) shows the equivalent DQ-frame model for the converter output current. The sub-index d , q and z_0 indicate the corresponding DQ-terms for their original and respective AC variables. As can be seen, when the transformation is applied, a cross-coupling exist between the d and q currents that is directly proportional to the fundamental frequency ω_0 . This means that the direct current i_d will be perturbed each instant there is a change in the quadrature current i_q , and vice versa.

Regarding the control, this new DQ-model with DC quantities allows the use of a PI controller for the output currents, and also provides the necessary information to tune the PI gains properly. In terms of tuning, usually the equations for the d and q channels are considered, while the use of the z_0 channel depends on the particular application or operating conditions. The PI controller will then deliver the required voltages e_d and e_q for controlling the i_d and i_q currents. Finally, these DQ-frame voltages must be reconverted

to their AC form by applying the inverse transformation matrix, $T_{abc} = T_{dqz}^{-1}$.

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} d \\ q \\ z_0 \end{bmatrix} = T_{abc} \begin{bmatrix} d \\ q \\ z_0 \end{bmatrix} \quad (4.26)$$

Figure 4.9 shows the control diagram for the output current in the DQ reference frame, where the z_0 is omitted since it is not for interest in this work. Two PI controllers are used, one for the d channel and the other for the q channel. As the current control is perform onto DC quantities, the current references also need to have this form. However, it is not necessary to use AC references and transform them into the DQ-frame. Instead, they can be given directly to the controller in their DC form. The current references i_d^* and i_q^* are useful for determine the power factor of the converter without employing shifted AC current references. Finally, decoupling terms are used in order to increase the performance of the controllers against the cross-coupling perturbations.

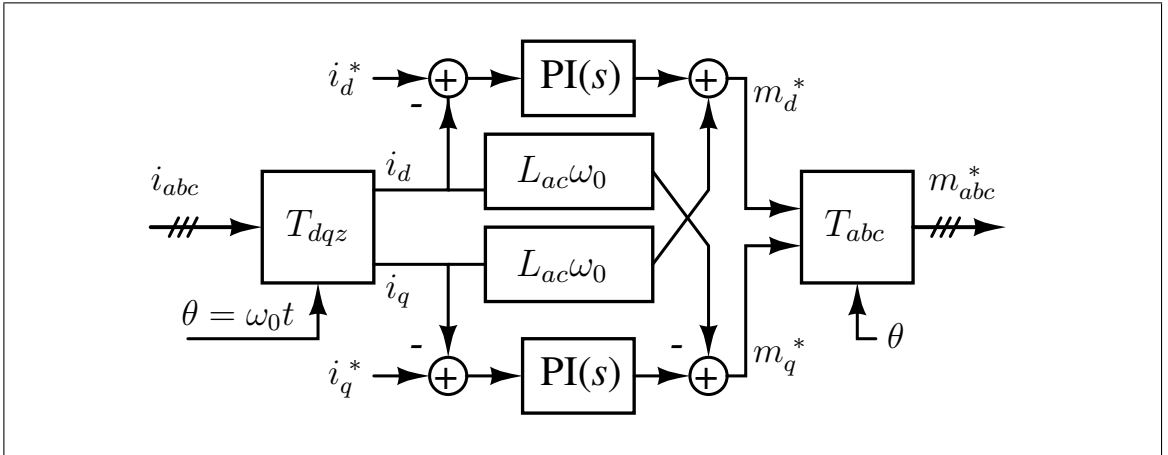


Figure 4.9. Output current controller diagram in the DQ-frame.

4.4.2. Circulating Current Controller

In the original topology of the MMC, the circulating current controller can be used to inject specific harmonics in order to decrease the voltage ripple on the SMs, trading

off efficiency and increasing the stress on the devices. But in the ALE-MMC, the DAB is employed to reduce the voltage ripple. Thus, injecting circulating current harmonics is not necessary and it is possible to suppress its second harmonic if the operation and conditions allow it.

Similar to the output current controller, different techniques can be employed in order to control the circulating current. Considering that it has a component with twice the fundamental frequency, in balanced conditions these currents are in negative sequence. The same control in the DQ-frame described previously can be employed, but swapping phases b and c due to their negative sequence. This would allow to inject currents more easily since DC references can be given. However, this method requires to know the circulating current angle θ_{iz} in order to perform the control, which may require more computation in order to obtain it.

Since in the ALE-MMC there is no intention of adding circulating current harmonics, this controller can be used to suppress its AC component. This will be named Circulating Current Suppression Control (CCSC) from now on, and its main objective is to reduce to zero the second harmonic of the circulating current. This is achieved by reshaping the modulated voltage in the arms stacks, avoiding the generation of voltage harmonics that give origin to the circulating current harmonics. A Proportional Resonant (PR) controller is chosen since it is, comparatively, easier to implement in this application as it does not require the angle θ_{iz} to work.

Nevertheless, unlike classical applications of PR controllers where the fundamental or resonance frequency are constant, in this applications the resonant frequency must vary with time. Then, the controller must have the flexibility to change its resonance accordingly, and it also needs an enough bandwidth around the target frequency in order to withstand frequency errors.

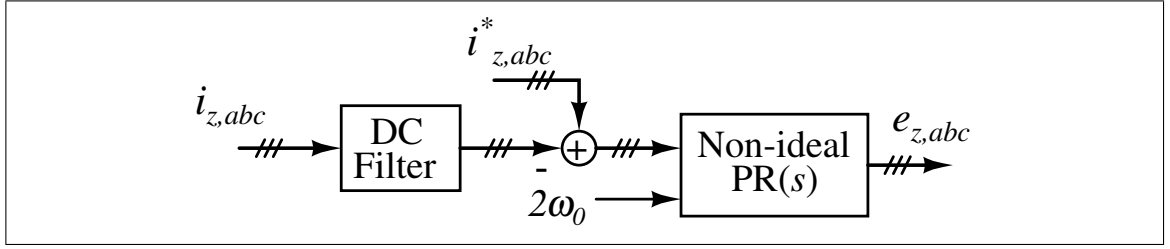


Figure 4.10. Proportional Resonant circulating current controller diagram.

Figure 4.10 shows the control diagram for the circulating current control. An ideal Proportional Resonant Controller has the following form:

$$H_{PR,ideal}(s) = k_p + k_r \frac{s}{s^2 + \omega_h^2} \quad (4.27)$$

where k_p and k_r are the proportional and resonant gains, respectively, and ω_h is the resonant frequency. This ideal PR has an infinite gain at the resonant frequency, which is desirable for a controller, but due to computation problems and its narrow bandwidth it is not a practical implementation. Instead, a non-ideal PR controller is preferred, which has the following form:

$$H_{PR,non-ideal}(s) = k_p + k_r \frac{s\omega_b}{s^2 + 2\omega_b s + \omega_h^2} \quad (4.28)$$

where ω_b is the cut-off frequency that defines the bandwidth ($\omega_b \ll \omega_h$). This version of the PR controller sacrifices the infinite gain at the resonance frequency, but it allows to be computed by the processor and also has a higher bandwidth for frequency errors.

The non-ideal PR controller is then chosen to perform the control, as shown in Figure 4.10. Nonetheless, the DC component of the circulating current may interfere with the proportional gain while controlling the second harmonic, if used directly. Thus, the controller must be complemented with a DC filter that eliminates this DC term of the measure. This DC filter can be a simple first order low-pass filter (LPF), or a second order LPF for better performance. The digital implementation can be seized and the cut-off frequency can be actively be updated in order to have the same performance and different frequencies. This way the PR controller will receive only AC values and the proportional gain will not act on the DC term. It must be noticed that the resonant frequency of

the controller must be twice the fundamental frequency, this is $\omega_h = 2\omega_0$. In order to implement the CCSC, one PR controller is implemented per phase, and all have zero current as reference ($i_{z,x}^* = 0$).

There are various methods to implement a non-ideal digital PR controller, and the computational burden required is not high. The digital implementation also helps to easily implement a controller with variable resonant frequency. So, given enough bandwidth and the digital implementation, the PR controller will not have problems to operate with variable fundamental frequency.

4.5. Effects of Circulating Current Suppression Control

In the classical MMC topology, circulating current presents a potential problem if not controlled properly, since it increases the arms RMS current and thus the converter loses (S. Li, Wang, Yao, Li, & Peng, 2015; Tu, Xu, & Xu, 2011). For some applications, it is desirable to suppress it to improve the performance, but in others, injection of it is implemented to operate the converter under certain conditions, such as low output frequency. In the ALE-MMC, the DAB helps reducing the voltage ripple together with the circulating current. However, in this topology, the suppression of the circulating current can improve the performance on the converter under certain conditions, not only in terms of efficiency but also in terms of the DAB performance. In order to analyze the different effects of suppressing the circulating currents, all the previous development are considered.

4.5.1. Arm Currents Harmonics

The first and immediate effect of suppressing the circulating current, which also applies for the classical MMC, is that it changes the harmonic content of the arm currents. As the second harmonic is eliminated, the arm currents are composed by the following

terms:

$$\text{CCSC Enabled} : \begin{cases} i_{u,x} = \frac{I_{DC}}{3} + \frac{i_x}{2} \\ i_{l,x} = \frac{I_{DC}}{3} - \frac{i_x}{2} \end{cases} \quad (4.29)$$

The CCSC makes the second harmonic amplitude equal to zero ($I_{2,z} = 0$), so only the DC appears on the circulating current. Consequently, through the arm currents will only flow a third of the DC current, plus half of the output current. The arm currents will then have only fundamental frequency AC components.

This elimination of the second harmonic translates into a lower RMS value on the arm currents and therefore into lower stress on the semi-conductor devices of the SMs. This reduces the conduction losses, but it may increase the voltage ripple in the SMs and change the switching losses of the SMs. Considering the variable frequency operation of the ALE-MMC and the circulating current resonance, the CCSC will have a higher impact when the fundamental frequency is close to half of the resonant frequency. In this condition, the CCSC will considerable reduce the conduction losses specially at higher output powers. Also, around the resonant frequency the circulating current may increase the voltage ripple due to the high values it can reach, and thus suppressing it may also reduce the oscillations, depending on what range is located the resonant frequency.

4.5.2. DAB Current Harmonics

The harmonic content of the DAB was derived previously in equation (4.22), in terms of the output and circulating current variables. From this equation, it is clear that the third harmonic terms depends on the circulating current AC amplitude $I_{2,z}$ and the mean voltage modulating amplitude. When the CCSC is disabled, or no control is implemented into the circulating current, the mean voltage modulating amplitude is zero $\hat{m}_z = 0$, and the DAB

current becomes:

$$\begin{array}{l} \text{CCSC} \\ \text{Disabled} \end{array} : \left\{ \begin{array}{l} i_{DC-DC} = \frac{I_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{I_o \hat{m}_o^2}{8} \cos(\varphi_L) \sin(\omega_0 t) \\ - \frac{I_{z,2} \hat{m}_o}{4} [\cos(\omega_0 t + \phi_{2,zx}) - \cos(3\omega_0 t + \phi_{2,zx})] \end{array} \right. \quad (4.30)$$

Here, the amplitude of the third harmonic is determined by the output voltage modulating amplitude, and the circulating current second harmonic magnitude.

When the CCSC is enabled the mean voltage modulating amplitude is non zero ($\hat{m}_z \neq 0$) and the AC magnitude of the circulating current becomes zero, this is $I_{2,z} = 0$. Then, the DAB current has the following form:

$$\begin{array}{l} \text{CCSC} \\ \text{Enabled} \end{array} : \left\{ \begin{array}{l} i_{DC-DC} = \frac{I_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{I_o \hat{m}_o^2}{8} \cos(\varphi_L) \sin(\omega_0 t) \\ - \frac{I_o \hat{m}_z}{8} [\cos(\omega_0 t + \varphi_L + \phi_{2,zx}) - \cos(3\omega_0 t - \varphi_L + \phi_{2,zx})] \end{array} \right. \quad (4.31)$$

In this case, the third harmonic magnitude depends on the amplitude of the output current I_o and the mean voltage modulating amplitude $\hat{m}_z$. However, the mean voltage modulating amplitude is considerable smaller than the output modulating amplitude when suppressing this current ($\hat{m}_z \ll \hat{m}_o$). This implies that $I_o \hat{m}_z \ll I_o$ and $I_o \hat{m}_z \ll I_o \hat{m}_o^2$ and consequently, the third term in equation (4.31) can be neglected. This result in an approximation for the DAB current when the CCSC is enabled with the following form:

$$\begin{array}{l} \text{CCSC} \\ \text{Enabled} \end{array} : \left\{ i_{DC-DC} \approx \frac{I_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{I_o \hat{m}_o^2}{8} \cos(\varphi_L) \sin(\omega_0 t) \right. \quad (4.32)$$

From (4.32), the DAB current will have only fundamental frequency terms when the CCSC is enabled, and its magnitude will depend on the output current amplitude I_o and the load angle φ_L . Considering this and the frequency response of the DAB, it will have a better performance when the CCSC is enabled, since it eliminates a third harmonic on it. This is particularly useful at high fundamental frequencies where the DAB performance is lowered, and the third harmonic frequency can reach considerably high values.

On the other hand, at low frequencies it may not be recommended to suppress the circulating current even if it improves the DAB performance. The first reason is because at low frequencies the DAB can have enough performance to transfer the power correctly between capacitors, even with the presence of the third harmonic. The second reason is that at low frequencies the amount of time in one fundamental cycle that the capacitors are active is higher, and this tends to greatly increase their voltage ripple. In these conditions, the circulating current helps to reduce these oscillations while working together with the DAB, so its suppression is not desirable.

Now with more insights about the behavior of the DAB at different frequencies, and also with the effects of the CCSC, the logic of enabling or disabling it can be determine. At low frequencies, it is desirable to have the AC circulating current in order to help reducing the voltage ripple. At high frequencies, the time the capacitors are active in one cycle is less, and thus the voltage ripple is lower. To this is added the fact the circulating current may enter in resonance for a given SM capacitance, so it is desirable to suppress the circulating current in this range, also reducing semi-conductor losses.

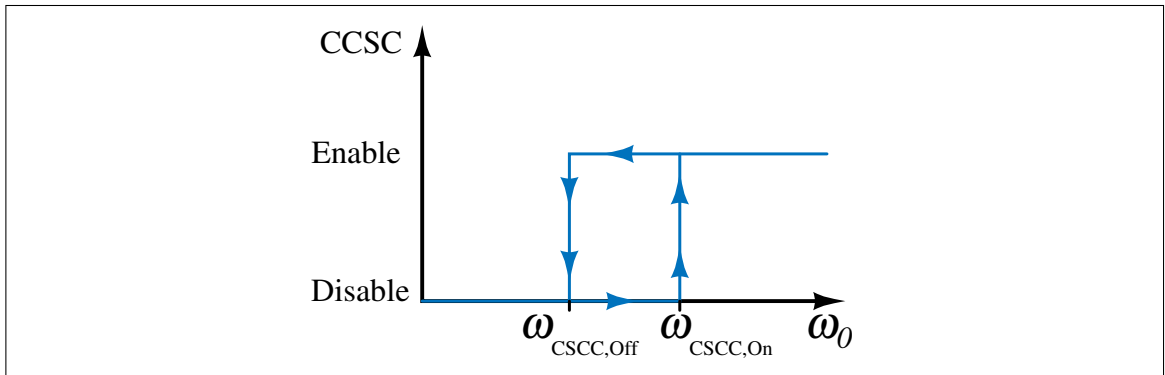


Figure 4.11. Enabling logic for the circulating current suppression.

Figure 4.11 shows the control logic for the CCSC, as function of the output fundamental frequency. A small range of hysteresis is recommended in order to avoid constant state transitions. $\omega_{CCSC,On}$ and $\omega_{CCSC,Off}$ are the turn-on and turn-off frequencies, respectively, that determines when the CCSC changes its state. These values will depend

on the whole operating frequency range, where the resonant frequency must also be considered when determining these values.

4.5.3. DAB Transformer Current Spectrum

The AC inputs of the DAB translates into AC currents of the same frequency in the DAB transformer, effect that is worsened at higher frequencies. The DAB current can be approximated with equation (4.32) when the CCSC is enabled. As the harmonic content in this case has only fundamental frequency components, it means that to the DAB transformer will be added a fundamental frequency current only, and not and additional third harmonic.

Based on the proposed operation for the CCSC, the third harmonic in the DAB transformer will disappear at frequencies above $\omega_{CCSC,On}$, so in this range the core losses will be lowered. At frequencies below $\omega_{CCSC,Off}$, the third harmonic will be present in the transformer, but in this range the magnitude of these harmonics will be lower, given an enough bandwidth for the DAB frequency response. The frequency gap to enable or disable the CCSC will depend on the particular application and operating conditions, as well as the converter parameters. It must be chosen in order to have a proper performance on both high and low output frequency range.

Summarizing, the logic for enabling the CCSC on Figure 4.11 correctly addresses the different requirements given an output frequency. Considering the behavior of all the variables and circuits, at low frequencies it is desirable to have the circulating current to help the voltage ripple. The DAB can have enough performance even with the third harmonic, since the input frequencies are not large. At higher frequencies, the circulating current can be suppressed since the voltage ripple is not to high, increasing the DAB performance and also reducing the transformer core losses. If the resonant frequency for the circulating current is in this range, then the conduction losses are greatly reduced, improving the efficiency of the converter.

4.6. DAB Power Estimation

In order to properly design the converter, an estimation of the power and currents handled by the different components must be determined. In this particular converter, the sizing of the DAB is an additional task that must be made in order to keep enough power margin and secure that the semi-conductors will withstand both voltage and currents required in the different scenarios. Since the DABs interlink upper and lower SMs, the voltage to which they are subjected is the same as that of the SMs, equal to $\frac{V_{DC}}{N_{SM}}$.

The current that the DABs handle must be analyzed with more detail. In operation with no CCSC, the current of the DAB is given by equation (4.30), which may be used for calculating the DAB current. However, determining the values of the second harmonic amplitude $I_{2,z}$ and its phase $\phi_{2,zz}$ is not direct and a more detailed analysis and calculation is needed.

Instead, the DAB current can be estimated with the CCSC enabled. In this case, the current i_{DC-DC} can be approximated with equation (4.32), that expresses it with known and simpler variables, unlike equation (4.30). The output current I_o and the output modulation signal amplitude $\hat{m}_o$ are easily obtained by the controller, while the load angle φ_L depends on the load or the desired power factor (depending on the application).

Given all this information and using (4.32), two curves of interest can be obtained. The first is the normalized DAB current with respect to an arbitrary output current (i. e. given an arbitrary load at an specific modulation index). This results in a function that depends on the output modulating amplitude and the load angle. Dividing (4.32) into this arbitrary current output current amplitude I_o yields:

$$r_{I_o, \text{DAB}} = \frac{i_{DC-DC}}{I_o} = \frac{1}{4} \sin(\omega_0 t - \varphi_L) - \frac{\hat{m}_o^2 \cos(\varphi_L)}{8} \sin(\omega_0 t) \quad (4.33)$$

$r_{I_o, \text{DAB}}$ can be interpreted as the percentage of the arbitrary output current (at the evaluated modulation index $\hat{m}_o$) that the DAB is transferring with the CCSC enabled. Logically, this percentage varies with time, but the interest is on the rms value $R_{I_o, \text{DAB}}$ that (4.33)

can reach. By applying the $\text{rms}()$ function to equation (4.33) for one fundamental cycle ($0 \leq \omega_0 t < 2\pi$), the curves in Figure 4.12 are obtained.

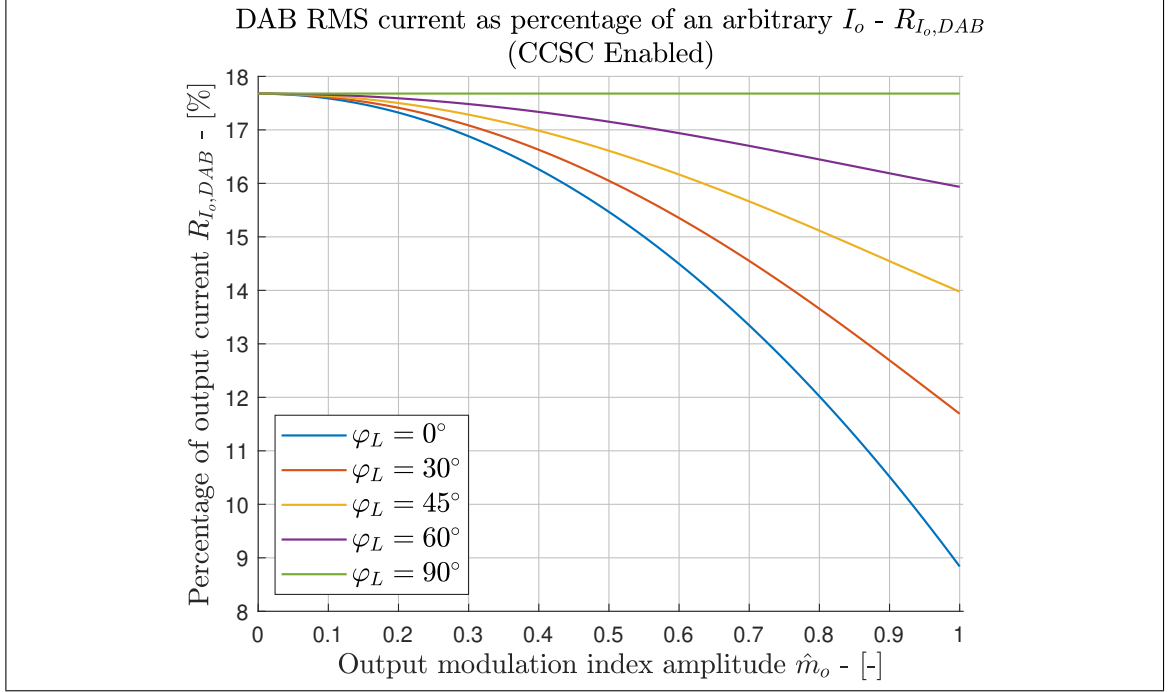


Figure 4.12. DAB current as percentage of an arbitrary output current with CCSC enabled.

As can be seen, the case where the DAB current has the largest RMS value occurs when the power factor is zero ($\varphi_L = \frac{\pi}{2}$), where it always has a current equivalent to 17.68% of the output current I_o . For higher power factors, the DAB current decreases quadratically as the output modulation index increases. When the power factor is 1, then the DAB current has the minimum RMS value possible for the modulation index range.

Even if the curves shows that at $\hat{m}_o = 0$ the DAB has a RMS current equal to the 17.68% of I_o , it must be considered that at this index value the output current is null, so the DAB will not be transferring any current.

Based on this, given a nominal or maximum converter output current $I_o^{\max}$, the DAB can be designed to transfer an RMS current of 17.68% of this value, and this will be enough

to cover the needed current for different modulation index and load angles. Obviously it is always good to have some current or power margin in order to have operation flexibility.

Although this estimation for the DAB current is based on enabling the CCSC, it still serves as start point to design the DAB even with the CCSC disabled in normal conditions. If the AC component of the circulating current is suppressed, it means that the DAB will have to increase the transferred current in order to compensate the absence of the circulating current, thus increasing its RMS current. Therefore, without CCSC the current transferred will have a lower RMS value and a different harmonic spectrum, and the peak current will not vary considerably from the case with CCSC, as the further simulations will show.

However, this estimation may not fit when the CCSC is disabled and the circulating current frequency is close to its resonant frequency $f_{z,res}$. In this case, even if the current nature is to balance the upper and lower stacks voltages, the resonance causes it to reach high values and increase the voltage ripple. Consequently, the DAB current increases accordingly and may exceed the values in Figure 4.12. The circulating current rise will depend on the equivalent series resistance of the leg R_{eq} , which acts as the damping factor. In order to avoid this, the circulating current resonant frequency must be in the high frequency range, so the CCSC can be applied and the resonance avoided, and then the above estimations will work.

The second curve is based on the percentage of the maximum current reachable given an specific load. The output current amplitude can be expressed as $I_o = I_o^{\max} \hat{m}_o$, where $I_o^{\max}$ is the current reached when the output modulation index is equal to 1 ($\hat{m}_o = 1$). Dividing (4.32) into $I_o^{\max}$ yields:

$$r_{I_o^{\max},DAB} = \frac{i_{DC-DC}}{I_o^{\max}} = \frac{\hat{m}_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{\hat{m}_o^3 \cos(\varphi_L)}{8} \sin(\omega_0 t) \quad (4.34)$$

Similar as the previous curve, applying the rms() function to (4.34) gives the DAB RMS current as the percentage of the maximum current reachable by the converter given a specific load.

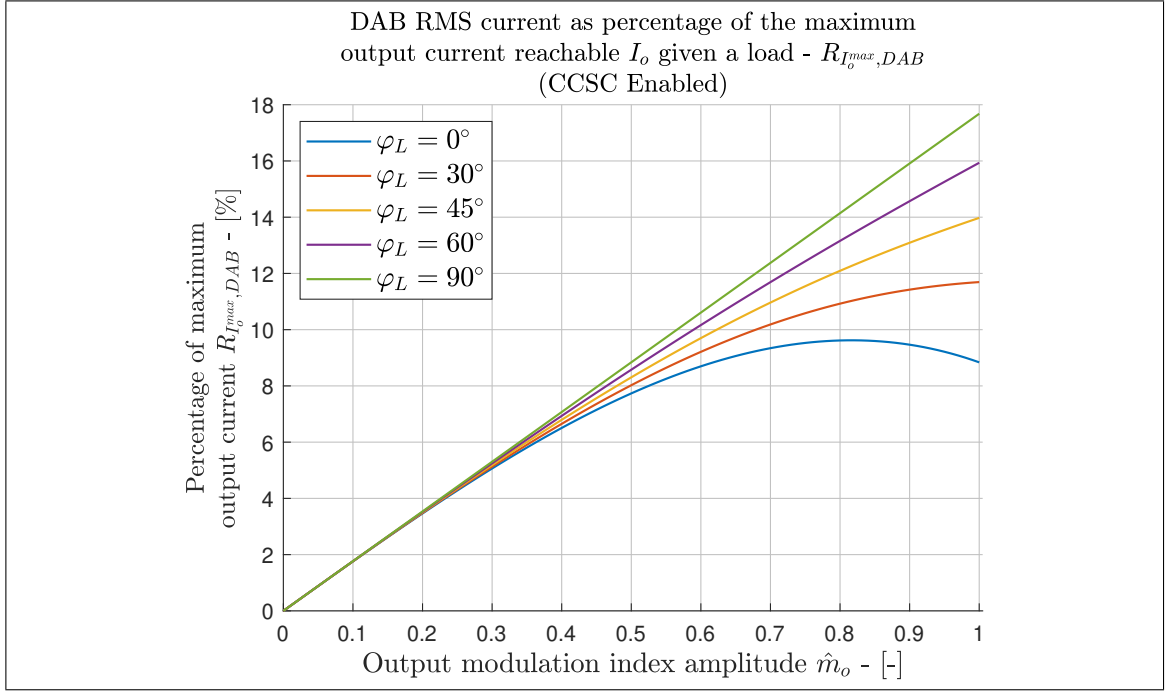


Figure 4.13. DAB current as percentage of the maximum output current reachable, with CCSC enabled.

As shown by the previous curve, Figure 4.13 also states that the case with higher current is when the power factor is zero. The main difference between Figure 4.12 and 4.13 is that the latter shows explicit that the DAB current will be zero when $\hat{m}_o = 0$, which is expected since there is no output voltage driving any current. For a given load, the DAB current will have a cubic behavior in relation to the modulation index $\hat{m}_o$. This cubic relation gets weaker when the power factor decreases, ending with a linear equation when $\varphi_L = 0$.

With the peak current determined, now it is possible to obtain an estimation of the power that the DABs will handle. This is simple considering that the DAB maintains a relatively constant value at its DC terminals, which is equivalent to $\frac{V_{DC}}{N_{SM}}$. Using equation (4.32), the instantaneous power the DAB handles can be expressed as:

$$p_{DAB} = \frac{V_{DC}}{N_{SM}} \frac{I_o}{4} \sin(\omega_0 t - \varphi_L) - \frac{V_{DC}}{N_{SM}} \frac{I_o \hat{m}_o^2 \cos(\varphi_L)}{8} \sin(\omega_0 t) \quad (4.35)$$

In order to have a better understanding of the powers being handled, it is desirable to relate the DAB power to the whole converter output power. Given that the DAB current is based on the currents flowing through the arms, it is better to compare its power to the apparent power of the converter. For a given load, the maximum apparent power achievable (when $\hat{m}_o = 1$) is given by:

$$S_o^{\max} = \frac{3}{2} \frac{V_{DC}}{2} I_o^{\max} \quad (4.36)$$

where $I_o^{\max}$ is the maximum current reachable ($I_o = I_o^{\max} \hat{m}_o$). Then, dividing (4.35) into (4.36) yields the DAB power as percentage of the maximum apparent power of the whole converter for a given load:

$$r_{S_o^{\max}, \text{DAB}} = \frac{p_{\text{DAB}}}{S_o^{\max}} = \frac{\hat{m}_o}{3N_{SM}} \sin(\omega_0 t - \varphi_L) - \frac{\hat{m}_o^3 \cos(\varphi_L)}{6N_{SM}} \sin(\omega_0 t) \quad (4.37)$$

This equation is similar to (4.37) and has the same behavior in relation to the modulation index. Then, applying the rms() function to this ratio, the curves in Figures 4.14 and 4.15 are obtained. These curves consider a constant DC-link voltage for the converter, so the greater the number of SMs, the lower their voltage.

As expected, for the same DC-link voltage the power handled by the DABs decreases for greater numbers of SMs. For a given number of SMs, the case where the DAB handles more power is when the power factor is null, shown in Figure 4.15. However, this case is only for exemplification since it is not a common operating condition and serves only for comparison and sizing.

In the case with full power factor (Figure 4.14), starting from $N_{SM} = 4$ the DABs handle less than 3.3% of the maximum apparent power, but values where $N_{SM} > 10$ will not make a considerable decrease on its power.

Even if the DABs power is reduced with greater SMs, the current they will handle does not depend on the number of SMs, which is a point to consider. This is because of the way the DAB operates, where it works as an alternative path for the arm currents to avoid charging or discharging the SM capacitors.

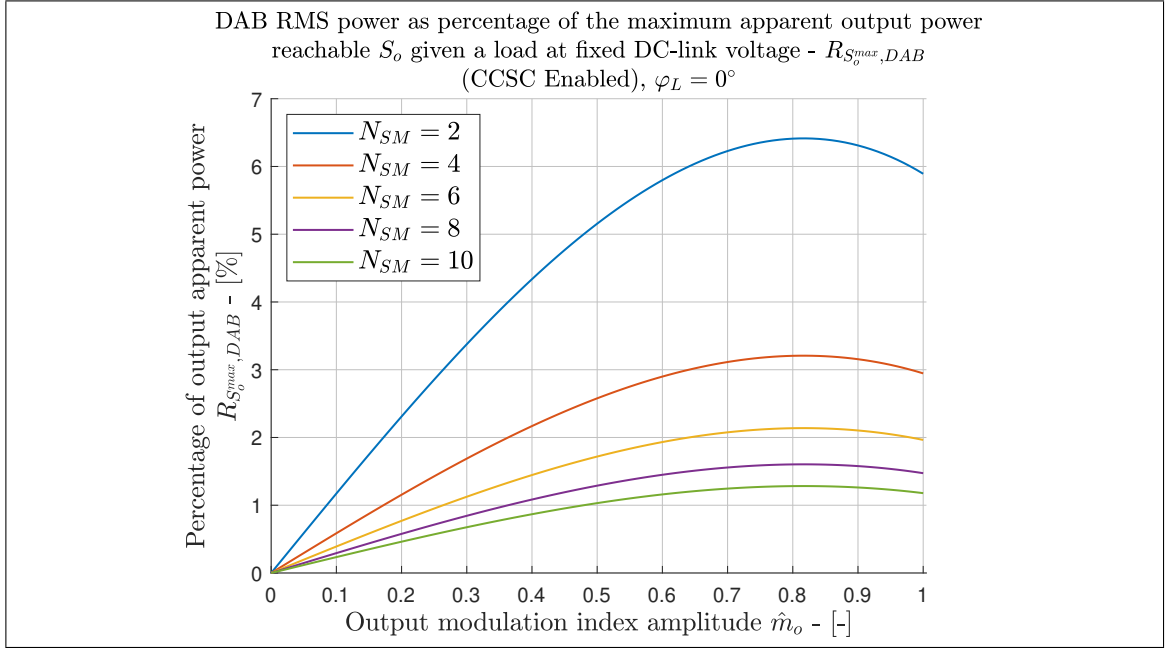


Figure 4.14. DAB power as percentage of maximum apparent output power for a given load ($\varphi_L = 0^\circ$, CCSC enabled).

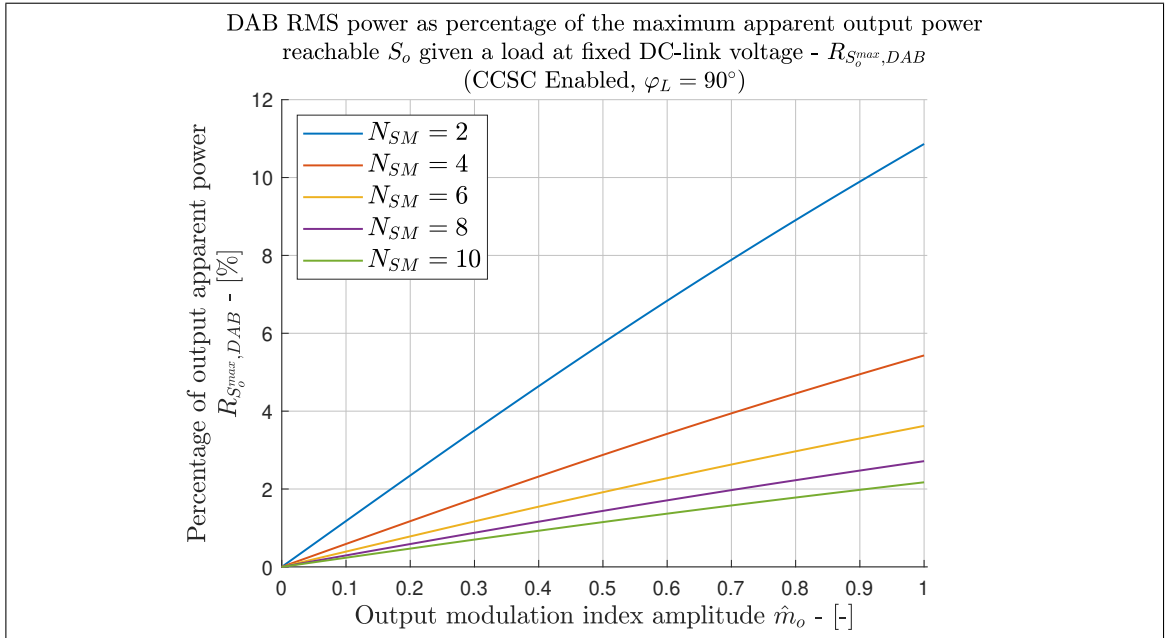


Figure 4.15. DAB power as percentage of maximum apparent output power for a given load ($\varphi_L = 90^\circ$, CCSC enabled).

Nevertheless, increasing the number of SMs for a given DC-link voltage reduces the switching losses of the semi-conductor devices. Considering the switching frequency of the DAB H-bridges, their switching losses are to consider, even with it operating in the full ZVS zone. Therefore, in order to get the better results, the trade-off between losses produced by adding a SMs (more semi-conductors devices) and loss decrease due to lower SM voltage must be considered.

4.7. Comparison with classical MMC

With the ALE-MMC topology and operation presented, it is desirable to compare the converter with the classical MMC. Chapter 2 discussed the classical MMC structure, its modeling and all the control scheme required for it to operate correctly. Therefore, a comparison between the two typologies is presented. Table 4.1 shows a comparison between the classical MMC and the ALE-MMC for the relevant aspects. A three-phase converter is considered and some quantities are given in terms of the number of SMs of a stack (N_{SM}).

Table 4.1. General comparison of a three-phase classical MMC and ALE-MMC.

Parameters	Classical MMC	ALE-MMC
High current semiconductors	$12 \cdot N_{SM}$	$12 \cdot N_{SM}$
Low current semiconductors	0	$24 \cdot N_{SM}$
Internal transformers	0	$3 \cdot N_{SM}$
SM Capacitance	1 to 5 mF	100 to 800 μ F
Arm Inductances	6	6
Current sensors	9	9
Voltage sensors	$6 \cdot N_{SM}$	0
Modulation technique	Any	PS-PWM
Overall control complexity	High	Low
Circulating current Injection	Complex	Not required
Circulating current Suppression	Simple	Simple
Arm energy control	Required	Not required
SMs sorting algorithm	Required	Not required
DAB Control	-	Open loop

Regarding the topology, the first great difference is the amount of semiconductor devices used in each converter. The classical MMC employs a large number of devices given its structure, but the ALE-MMC uses 200% more devices than the original topology. It can be considered that six devices are used per SM in the ALE-MMC, two for the Half-Bridge and four for the DAB H-Bridge. Taking into account the current handled by the DAB, the extra semiconductors can be rated for lower current, so the cost is not excessively increased. Anyways, the amount of semiconductors may raise concerns about the reliability of the converter, but considering that the ALE-MMC is intended for the low voltage range, even lower voltage-rated devices can be used, reducing these concerns. Besides the extra devices, there is also the addition of high-frequency transformers for the DAB. These can affect the efficiency of the converter, but as seen previously, they handle a small portion of the converter apparent power. Also, there were presented methods for the DAB to reduce losses and increase its performance, added to the fact that it is operating practically always in ZVS condition.

Another highlight is the size of the SM capacitance. The incorporation of the DAB allows to transfer the power from an upper capacitor to another, so the excess of charge on them is avoided in the ALE-MMC. Consequently, the capacitance can be significantly reduced compared to the classical MMC. This saves a considerable space in the SMs, which compensates the addition of DAB between SMs. To this is added the fact that no voltage sensors are needed in the ALE-MMC, which saves more space in the SMs design and also reduces the measurement system complexity.

Table 4.1 also shows a comparison about the control requirements, and Figure 4.16 shows the control structure of both converters, where significant differences appear between them. The first difference is that the MMC can use several modulation methods, and the other controllers adapt to it. The ALE-MMC requires the PS-PWM in order to operate, since it produces an equal power distribution and behavior among the SMs of the upper and lower stacks.

The highlighted difference is the dedicated SMs capacitors voltage control. The classical MMC employs several sensors ($6 \cdot N_{SM}$) and control loops in order to balance the SMs voltages, which includes the arm energy control and the sorting algorithms for the individual SMs capacitors. This translates into a complex measurement and information system that must be handled by the controllers, increasing the required computational burden of the topology. On the other hand, the ALE-MMC does not require voltage sensors, and the regulation of the SMs voltage is made through an open-loop control, needing only current measurements. In other words, the arm-currents based open-loop control for the DAB replaces all the SMs and leg voltage control and algorithms of the classical MMC. This results in an appreciable reduction on the measurements and control complexity, requiring only current values to perform the control. Regarding the circulating current, while in the classical MMC it is usually injected to reduce the voltage ripple (if not suppressed), in the ALE-MMC the circulating current is only suppressed depending on the fundamental frequency, and thus does not exist a reference coming from the arm energy controller.

Another consideration is about the operating capabilities of both converters. At low frequencies the voltage ripple on the capacitors increases significantly due to the time they are active. Thus, the chosen SM capacitance of the classical MMC may not ensure a safe ripple in these conditions, specially if it is used as medium-voltage speed drives. However, as the ALE-MMC employs the DAB for power transfer between SMs, it can withstand a very low frequency and even a zero-frequency (or DC) operation while ensuring a low voltage ripple, as the next chapters will show.

Even if the comparison highlighted the advantages and disadvantages of each converter, it must be considered that the intended applications for each are different. The MMC is considered mostly for HVDC transmission with fixed frequency, and also for medium-voltage speed drives, where hundreds of SMs are considered per arm stack. The conditions in these scenarios (such as available space, project costs, SMs quantities, etc) are different to the conditions in the low-voltage range, where the ALE-MMC is intended

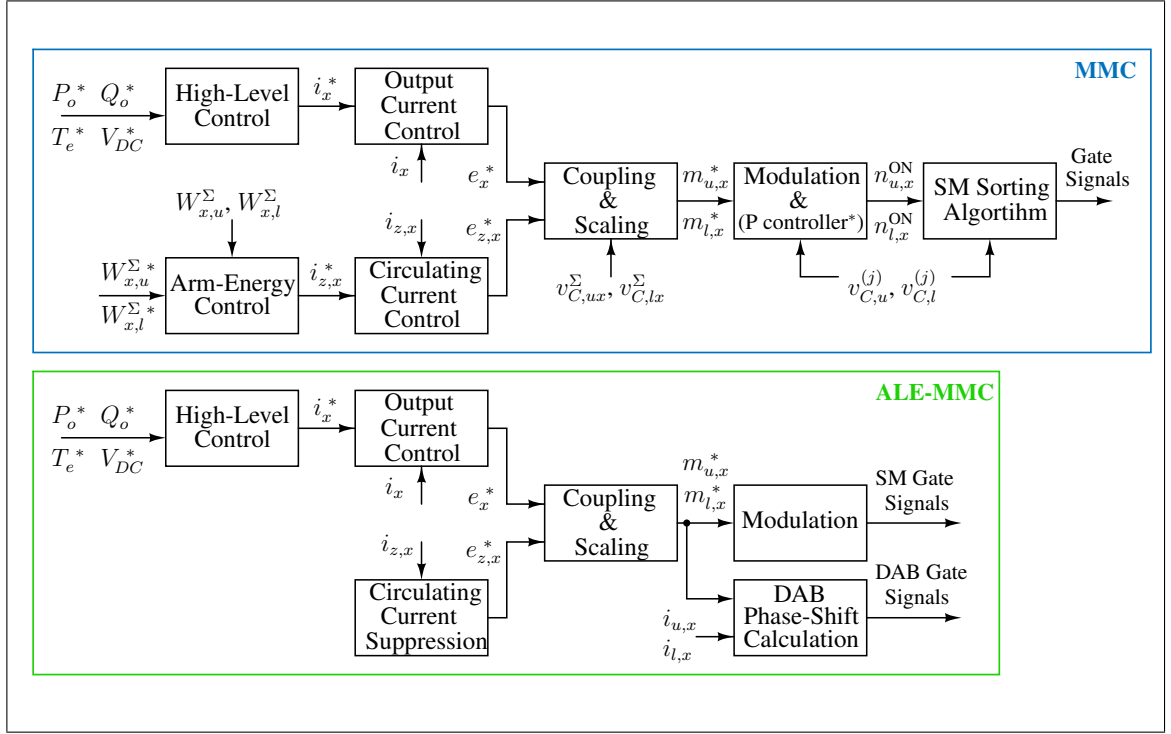


Figure 4.16. Control scheme comparison between classical MMC and ALE-MMC.

to operate. This is though to work in a variable frequency range with a lower number of SMs per stack due to the limited space. Therefore, the comparison is also made for showing how the classical MMC was adapted to operate as a low-voltage speed drive, and how these changes fulfilled the different requirements.

Finally, in order to validate the ALE-MMC as a viable solution for low-voltage power applications, it must be comparable to other actual low-voltage solutions, such as the two-level inverter or NPC topologies. The two-level inverter has the advantage of being extremely simple in terms of construction and control, and is well-known and implemented solution in the industry. However, it is subject to high losses and THD due to the larger voltage the devices withstand, lowering efficiency and increasing the cooling requirements. On the other hand, the NPC converter lowers the THD and increases efficiency, but it requires complex control to maintain the floating capacitor under proper conditions. Moreover, it is limited to three or five output voltages levels.

In this sense, it is of interest of having higher voltage levels solutions in the low voltage range since their benefits are already demonstrated. Thus, the ALE-MMC allows to bring these benefits to the low voltage range by making some modifications to the original topology. The benefit of modularity is still maintained, but the main advantage is the improvement on the power quality. This reduces the stress on both the energy source and the load, and can increase the lifespan of different equipment, but can also improve the efficiency of the system. Efficiency is a major factor to consider, and its determinant on whether the solution is viable or not, but a comparable performance can be expected given the results of the MMC in other applications. Nevertheless, what will determine if the ALE-MMC is viable is the actual implementation of the converter and full-power experiments, evaluating variables such as efficiency, power quality, costs, cooling system, etc., and comparing them with the other solutions.

The following chapters will detail the results of a three-phase ALE-MMC simulation, and of a single-phase low scale experimental prototype. They will serve as an initial assessment and validation of the converter principles and concept. Hence, these initial results will open the way for higher power and full operating conditions tests for future works and determine the actual performance of the ALE-MMC compared to other solutions.

5. SIMULATION RESULTS

In order to verify all the analysis developed in the previous chapter, a three-phase converter is simulated in PLECS software with the parameters shown in Table 5.1.

Table 5.1. Simulation parameters.

Variable	Symbol	Value
DC-link voltage	V_{dc}	500 [V]
Number of Cells per Arm	N_{SM}	10 [-]
Sub-Module Capacitance	C_{SM}	220 [μ F]
DAB Total Inductance	L_s	6.8 [μ H]
Arm Inductance	L_{arm}	200 [μ H]
Line to line output voltage	V_{LL}	220 [V]
Load Resistance	R_{Load}	6 [Ω]
Load Inductance	L_{Load}	900 [μ H]
Half-Bridge switching frequency	$f_{sw,MMC}$	10 [kHz]
DAB switching frequency	$f_{sw,DAB}$	50 [kHz]

A DC-link voltage of 500 V and 10 SMs per stack are chosen, which means an average voltage of 50 V in each SM. Note that the SM capacitance C_{SM} is considerably lower than the typical values for the original MMC, which are from the order of mF. With these values, the average resonant frequency of the circulating current, given by equations (4.15) and (4.16), is approximately $f_{z,res}^{average} \approx 1.199$ kHz. Hence, the resonance will be produced when the fundamental frequency f_o is around 599.5 Hz approximately.

The simulations will show the converter operating in different scenarios, detailing the relevant variables for each case.

5.1. Standard Operation

These simulations show the ALE-MMC operating at different frequencies without controlling the CCSC, in order to show its basic operation and behavior. Figure 5.1 shows the operation of the ALE-MMC at 5 and 50 Hz, while Figure (5.2) shows the results for 400 and 700 Hz. In all cases the peak output current is $I_o = 25$ A.

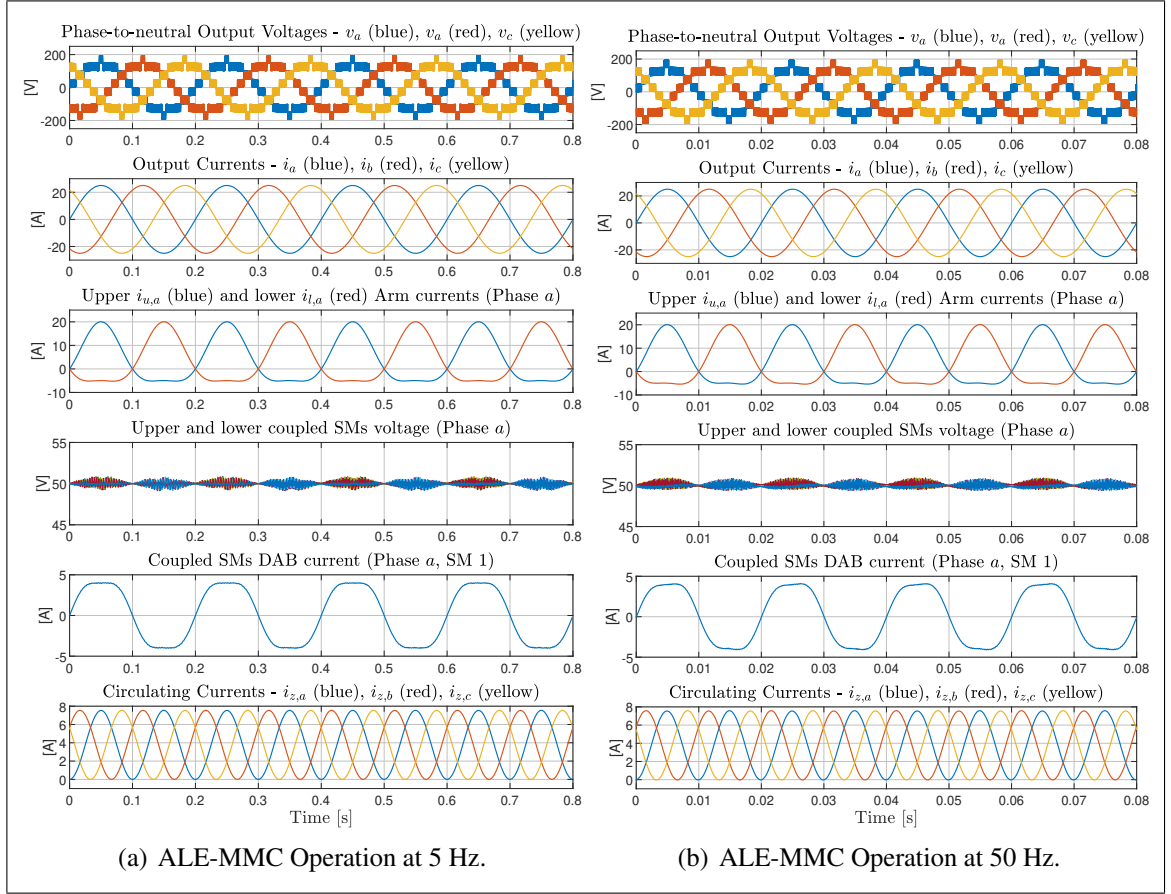


Figure 5.1. ALE-MMC operation at (a) 5 Hz and (b) 50 Hz. $I_o = 25$ A.

At low frequencies (Figure 5.1), the voltage ripple in the SMs is practically constant, with an amplitude lower than 1% of the DC value. In these conditions, the DAB has a better performance compared to higher frequencies, so the power transfer works correctly. There is no a significant difference in the voltage ripple between 5 and 50 Hz, and neither on the arm or DAB current spectrum.

The classical MMC topology can have problems operating at very low frequencies if no additional control logic is added, since the SMs voltage ripple would be greater given the time the SMs are active. There exists various mitigation strategies to overcome this problem. Injection of sinusoidal circulating current harmonics (manipulating the arms mean voltage) (Debnath, Qin, & Saeedifard, 2015), and injection of square wave circulating currents in the converter legs (Hagiwara, Hasegawa, & Akagi, 2012) allows to

maintain safe levels of SMs voltage ripple under low frequency operation. However, this produces a circulating current with magnitudes comparable to the actual output current, so the power losses and components size and ratings are increased. In the ALE-MMC however, no injection of circulating current neither additional control logic is needed, since the DABs open loop control is enough to maintain the SMs voltage in a very safe level.

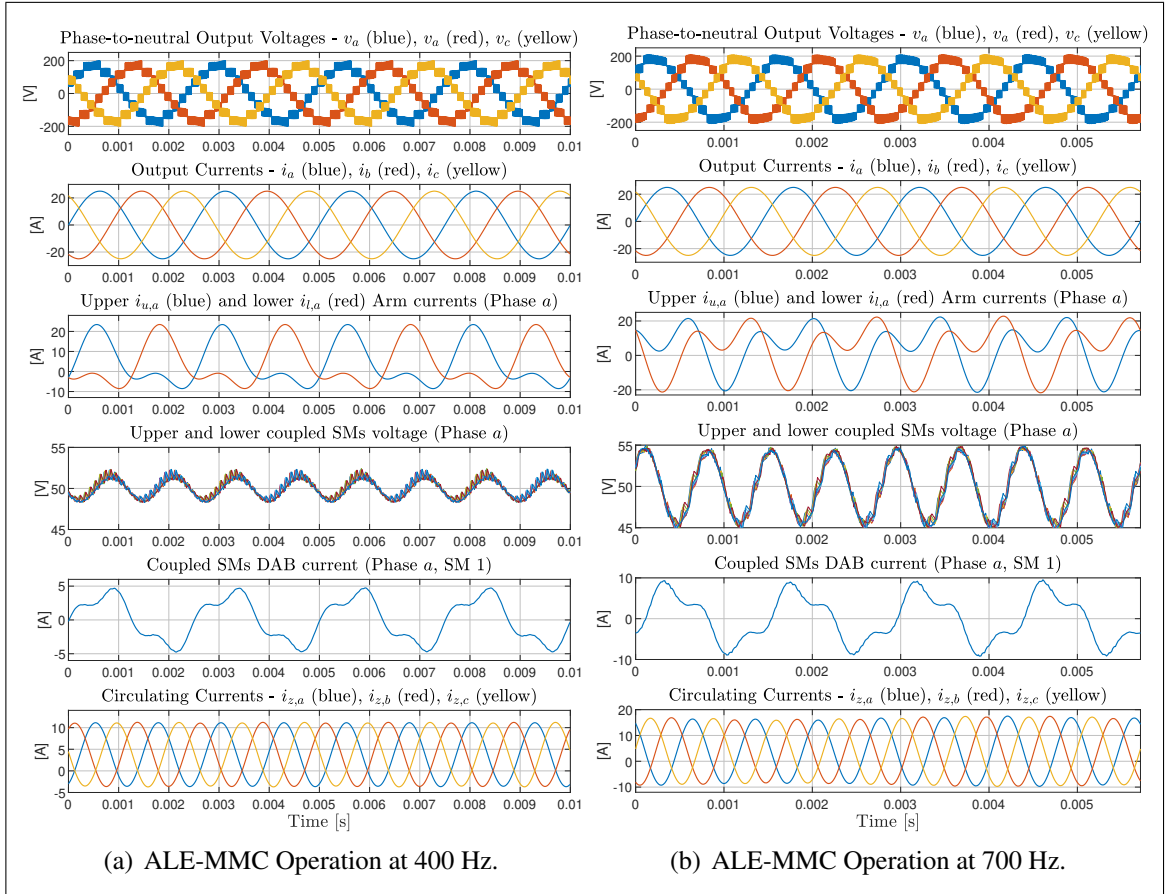


Figure 5.2. ALE-MMC operation at (a) 400 Hz and (b) 700 Hz. $I_o = 25$ A.

Operating at higher output frequencies, noticeable changes in the different converter waveforms (Figure 5.2). It can be seen how the DAB current spectrum changes due to variations in the currents and modulation index angles. The voltage ripple starts to increase at higher frequencies, even when it should decrease. The reason is because the circulating

current is close to its resonance (1.19 kHz), so its AC value starts to increase, which can be seen comparing with the cases in Figure 5.1. The closest case to the resonance is Figure 5.2(b), where the AC circulating current has more than twice the values in the low frequency cases. This results in the DAB handling more current, as anticipated in the previous chapter. Another undesirable effect at this frequency range is that the DAB has a lower performance due to its frequency response, where its power transfer and transformer currents are affected. The effect of the resonance is also seen in the arm currents, which translates into more currents stress on the semiconductor devices. This reinforces the idea of activating the CCSC in the high frequency range, specially when it is close to the resonant frequency.

Although the AC circulating current increases, the voltage ripple still has an amplitude of 10% of the DC value. Even the output currents are not deformed in all the frequency range, so the converter can be considered to operate properly even with resonance involved. It is necessary to highlight the fact that DAB maintains an equal voltage on the coupled upper and lower SMs, which allows it to operate into full ZVS zone. This is an expected effect since the DAB transfer any excess of charge from one capacitor to another, so the voltage difference between them is zero.

In order to verify the behavior of the ALE-MMC in variable frequency operation, Figure 5.3 shows a frequency transient from 50 to 700 Hz in 0.2057 s with constant output current equal to $I_o = 25$ A. The converter operates normally in the low frequency range, where the voltage ripple and the circulating current slowly increase as the fundamental frequency goes higher. Before approaching the frequency at which the circulating current resonance is produced, all the variables have a normal behavior.

Once the fundamental frequency is around the critical frequency (shown in red, approx. 600 Hz), the circulating current enters in resonance and quickly increases its AC value. The resonance affects all the other variables, in particular the SMs voltage and the arm currents, where the latter reach dangerous values even if the output current is relatively constant. The natural balancing is lost and instead the capacitors absorb the

resonance current and consequently increases the voltage ripple. This also produces the DAB to handle higher current, and may exceed its maximum power transfer. As the SMs voltages become unstable, the output current is also affected and cannot be maintained properly. In summary, operation around the critical resonant frequency leads the converter to a possible unstable operation, depending on the magnitude of the resonance and the actual output power of the converter.

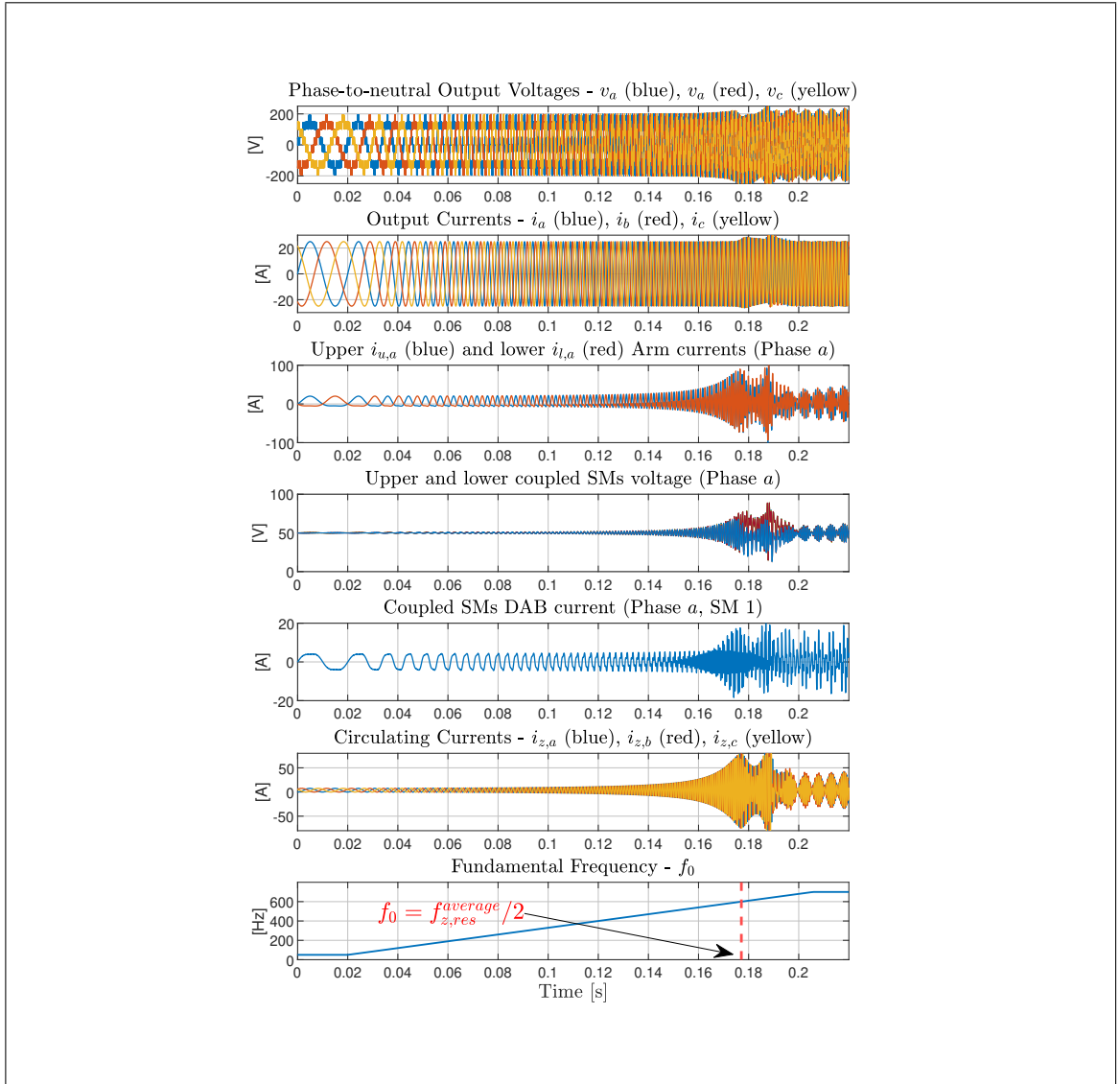


Figure 5.3. ALE-MMC operation with frequency ramp from 50 to 700 Hz.

However, it must be considered that this simulation has idealities and it does not consider parasitic effects of the real converter, such as equivalent series resistance or semi-conductor on-state resistance. These parasitic effects actually prevent the circulating current to reach extreme values in resonance, acting as damping quantities. So, in the real converter the overall effects of the resonance will not be as severe as in the simulation, and it may operate properly in the resonance range depending on other factors, as will be shown in the experimental results. Nevertheless, this simulation shows that around the resonance undesirable effects occurs that do not contribute to the performance. In conclusion, at higher frequencies it is desirable to suppress the circulating current in order to stabilize and increase the performance.

5.2. Circulating Current Suppression

Now that the standard operation was shown and verified, the operating with Circulating Current Suppression Control is simulated. For this, three PR controllers are used, one for each phase. The digital implementation of the PR controllers actively adjust the target tuning frequency so it is equal to twice the fundamental frequency of the converter ($2\omega_0$).

Figure 5.4(a) shows the case for $f_0 = 100$ Hz with an output current of $I_o = 25$ A. At the moment the CCSC is enabled, it can be seen that the control is not totally smooth and it takes some time to stabilize the circulating current. The reason it can not control properly the AC part of the current is because the voltage ripple increases. Trying to suppress the circulating current at low frequency eliminates the natural balancing of the upper and lower capacitors, so they absorb more charge and increase their ripple. Moreover, the time the SMs are active within one fundamental cycle is considerable at lower frequencies. The DAB, in this situation with CCSC enabled, tends to equal the voltages of the coupled capacitors but it can not avoid that more charge is being absorbed by the capacitors, so a voltage ripple is generated. Thus, the CCSC does not improve the performance around this frequency range.

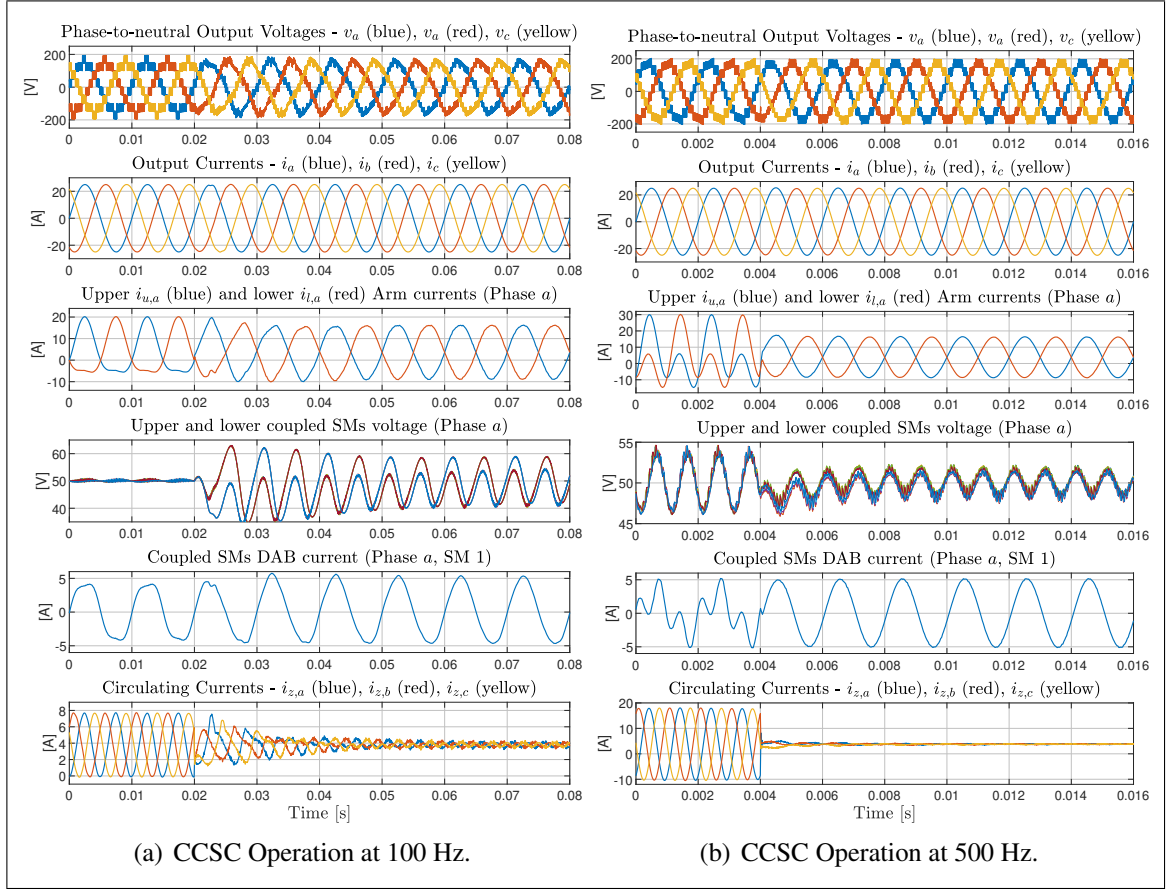


Figure 5.4. CCSC operation at (a) 100 Hz and (b) 500 Hz. $I_o = 25$ A.

On the other hand, the effects of enabling the CCSC at higher frequency are notably different, as Figure 5.4(b) shows. At this frequency the circulating current is relatively high due to the resonance, and this produces a small increase on the SMs voltage ripple, but the converter still operates properly. When the CCSC is enabled, the circulating current AC is smoothly suppressed and only the DC term is left. As predicted with equation (4.32), the CCSC produces the DAB to handle only a fundamental frequency component. The peak and RMS value of the arms current are considerable lower, so the SM semi-conductor devices withstand less current stress and conduction losses are lower. The voltage ripple of the SMs is also lowered since the resonance is damped, but also because the DAB has a better performance since a third harmonic was suppressed. Even if the CCSC eliminates the natural balancing given by the circulating current, the voltage ripple does not increase

in comparison to the low frequency range. This is because of the lower time the SMs are active at high frequencies during one fundamental cycle. This makes them absorb less charge and avoids dangerous levels, while the DAB maintains both upper and lower voltages in the same value.

These results confirm that it is convenient to enable the circulating current control at high fundamental frequencies, as proposed in Figure 4.11. In order to simulate this control, Figure 5.5 shows a ramp from 50 to 700 Hz in 0.2057 s maintaining an output current of $I_o = 25$ A, but enabling the CCSC from $f_0 = 400$ Hz. Similar to the case in Figure 5.3, at low frequencies the converter has a good performance, maintaining a low voltage ripple on the SMs. However, before entering into the circulating current resonance range, the CCSC is applied in order to avoid reaching high values. The consequence is that no resonance is produced since no circulating current is flowing. Then the behaviors in Figure 5.3 do not happen in this case and the converter operates correctly. In addition to the reduction of the current stress on the semi-conductor devices, the voltage ripple is maintained lower than a 5% approximately of the DC value for the whole range. The output current is maintained perfectly at 25 A for all the frequencies thanks to the low ripple, and the DAB current has no major variation in the peak current transferred.

Summarizing, the CCSC greatly solved all the problems of the ALE-MMC operating at high frequencies and in the range of the circulating current resonance. It improves the performance of the DAB and avoids the circulating current to reach high values, which secures the well behavior of all the other variables. On the other hand, having the circulating current seems to be beneficial since it helps to reduce the voltage ripple together with the DAB. In this range the DAB has a higher performance too, so the power transfer is more effective which is reflected in the low ripple.

Another aspect to highlight of the CCSC simulations, is the peak current the DAB handles. In Figure 5.4(b), the conditions are that a current of 25 A is achieved with a modulation index of $\hat{m}_o = 0.673$ and the load angle is $\varphi_L = 25.23^\circ$. Now evaluating these values in equation (4.33) or in the curves from Figure 4.12, yields that the DAB

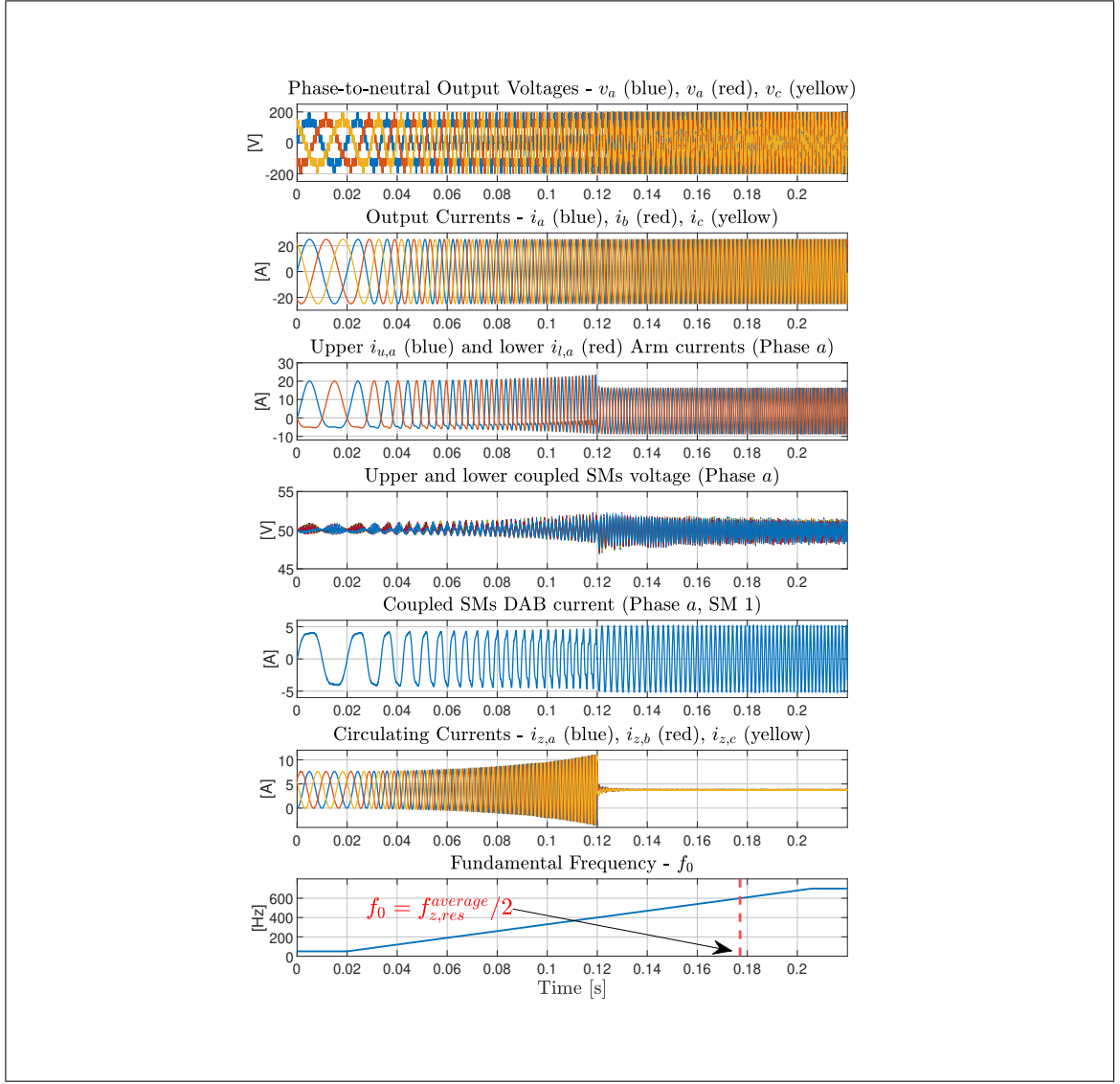


Figure 5.5. CCSC operation with frequency ramp from 50 to 700 Hz.

RMS current will be equal to 14.48% of the output current. This means that the DAB will theoretically handle a peak current equal to $i_{\text{DAB}}^{\text{peak}} = 25 \cdot \sqrt{2} \cdot 0.1448 = 5.12 \text{ A}$, which fits well with the actual current in the simulation. This value is actually close to the peak current in the case from Figure 5.4(a) at 100 Hz, even when there is a higher voltage ripple.

Considering the frequency ramp of Figure 5.5, it can be notice that the DAB current amplitude is practically constant in the whole range where the CCSC is enabled. On the

other hand, with the CCSC disabled at lower frequencies, the peak value is actually lower than the case with the suppression enabled. This means that, as long as the circulating current resonance is avoided, the estimations and curves obtained for the DAB peak current (or power) do fit with the simulation scenarios. Hence, these can be used as start point to design the DAB and properly address the converter requirements.

5.3. Start-Up or DC Output Current

An important requirement for variable-speed drives is its capability to drive full output current (or output torque) at zero-frequency, or at the motor start-up. In the classical MMC, it is unsuitable to have a DC output current for a long time without additional control and strategies. This is because one of the leg stacks would constantly absorb the DC current flowing, increasing the voltage and ending up affecting the performance or damaging the semi-conductor devices. Modulating a square wave in the arms mean voltage, and thus injecting a square wave circulating current, the SMs voltages can be maintained with low ripple even when DC output current is being driven (Hagiwara et al., 2012). However, similar to the low-frequency operation case strategies, this involves increasing the circulating current magnitude to very high levels, increasing power losses and sizing of the components.

As the ALE-MMC is intended to operate with variable frequency, it is desirable or required to operate it with zero-frequency. Figure 5.6 shows the simulation results for a ramp from 0 to 25 A (in the DQ frame) for different instantaneous angles (constant $\omega_0 t$). As can be seen, the converter operates properly with zero-frequency maintaining the capacitors practically at their DC value. In this topology, the DAB acts as an alternative path for the arm currents, so even when a DC current is present, it can flow through the DABs without constantly charging the SMs capacitors. This shows that the converter can operate at zero-frequency while driving the same output currents as it would do with a non-zero frequency, so it can be employed at start-up moments or when a null frequency is needed (for example, for maintaining the position). It is worth mentioning that no

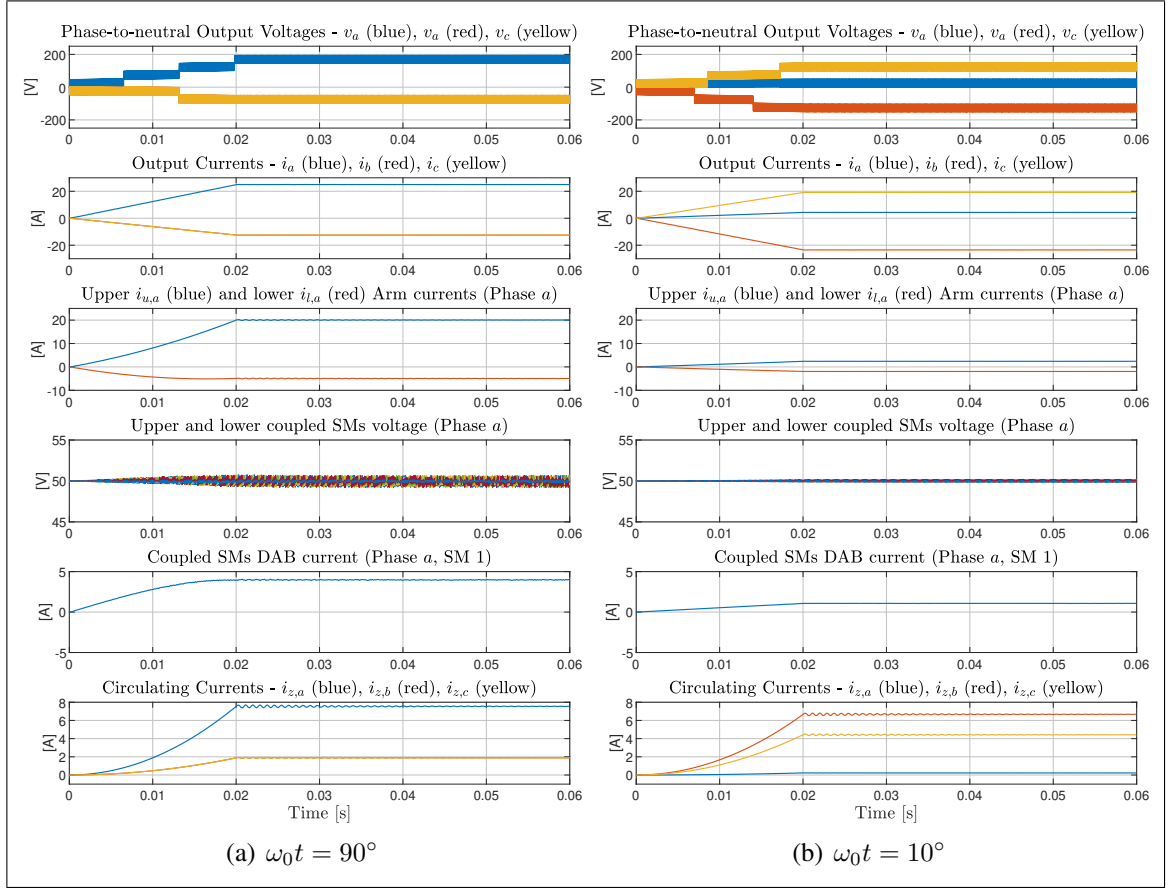


Figure 5.6. ALE-MMC operation at zero-frequency, with $I_o = 25$ A.

additional control or current injection needs to be implemented, contrary to the classical topology. Finally, the DAB has full performance in these conditions since it is transferring a DC current with a DC voltage value on its terminals.

5.4. DAB Transformer Current

As stated in the Chapter 4, the AC control inputs on the DAB are reflected on its transformer current, due its low-pass behavior. The higher the frequencies, the higher the magnitude of the currents with the input frequency in the transformer, depending on its bandwidth.

Figure 5.7 shows the harmonic spectrum of the DAB transformer current at $f_0 = 50$ Hz, with the CCSC disabled and $I_o = 25$ A. It shows the harmonics around the nominal switching frequency of the DAB (50 kHz), and the harmonics around the fundamental output frequency of the converter. As expected, the fundamental frequency harmonics have a smaller magnitude compared to the nominal ones. Thus, in this range the DAB operates with a good performance, and this improves as the frequencies goes lower. Enabling the CCSC in this range will not improve significantly the performance, on top of which the voltage ripple rises if it is enabled.

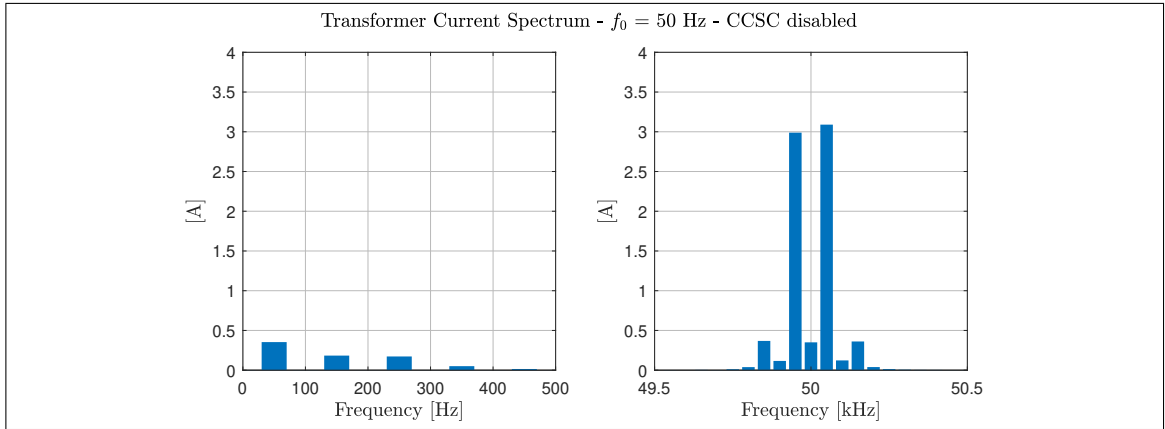


Figure 5.7. DAB transformer current spectrum at $f_0 = 50$ Hz (CCSC disabled, $I_o = 25$ A).

Figure 5.8 shows the transformer current spectrum for a converter output frequency of 400 and 500 Hz with an output current of 25 A. As it follows from equation (4.30), and considering the bandwidth of the DAB, the fundamental frequency and a third harmonic have a high magnitude in the transformer current. The third harmonic is critical since it can easily surpass the cut-off frequency and the undesirable effects will be stronger.

The third fundamental harmonic in the DAB current comes from the circulating current second-harmonic AC term, as equation (4.30) states. Suppressing this AC term in the converter will eliminate this third harmonic in the DAB current, and as equation (4.32) shows, the DAB will handle only a fundamental frequency component. From Figure 5.8,

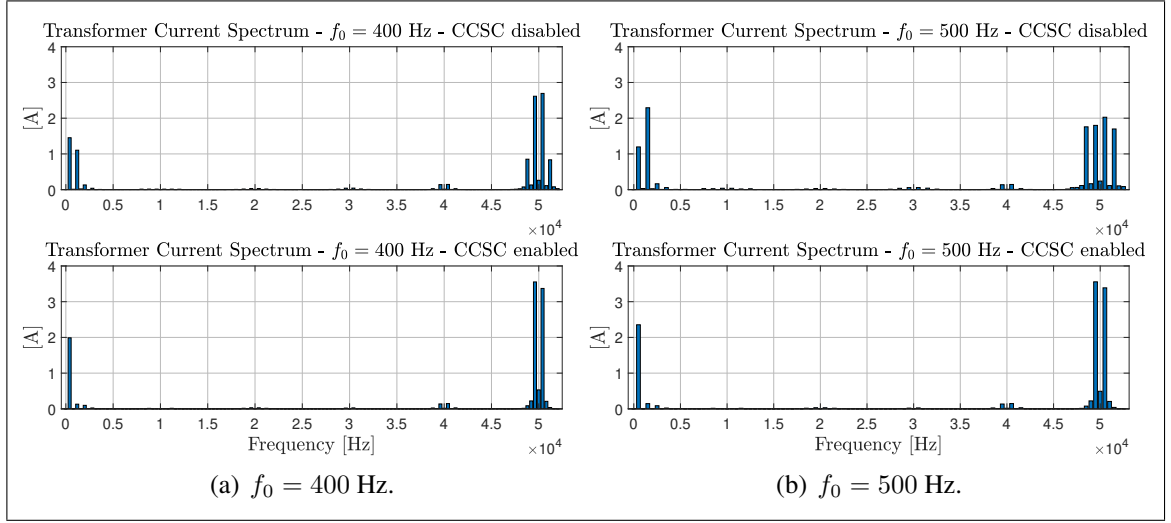


Figure 5.8. DAB current spectrum at (a) 400 Hz and (b) 500 Hz. $I_o = 25$ A.

once the CCSC is enabled the third harmonic disappears from the transformer current and the nominal frequency values (around 50 kHz) actually increase their magnitude. This means the DAB and its transformer will have a higher performance, reducing losses and improving the power transfer. The fundamental frequency harmonic also increases its magnitude due to the fact that, in normal conditions, the DAB has to handle a higher current to maintain a low voltage ripple. However, it is convenient to have only a fundamental frequency harmonic without a third one, since the effects of reduced performance (due to the low-pass filter behavior), hysteresis and core losses are lower.

These results shows that another benefits arises with the CCSC at high frequencies, reducing the low-harmonic stress on the DAB transformer. Nevertheless, due to the presence of a permanent fundamental frequency component, the DAB and its transformer should be designed to withstand these low-frequency harmonics given an operation range.

5.5. Losses Estimation

Considering the amount of semi-conductor devices and the switching frequency of each sub-circuit, it is desirable to have an initial estimation their losses. A thermal model

of the 100 V, 300 A IPT020N10N3 Infineon MOSFET was implemented in PLECS for both the DABs and the SMs.

Figure 5.9 shows the estimated semi-conductor losses at different fundamental frequencies, with the CCSC disabled and enabled. Both conduction and switching losses (turning on and off) are considered, from all the SMs and the DAB Half-Bridges. The results shows that at lower frequencies the losses are higher when the CCSC is enabled. This is explained by the fact that the voltage ripple increases in these conditions, increasing the switching losses of the devices. On the other hand, at high frequencies (and close to the circulating current resonance range), the losses are higher with the CCSC disabled. This is due to a mixed effect between the increase in the voltage ripple and in the circulating current amplitude. Suppressing the circulating current in this range greatly helps to reduce losses since both voltage ripple and arm current are reduced.

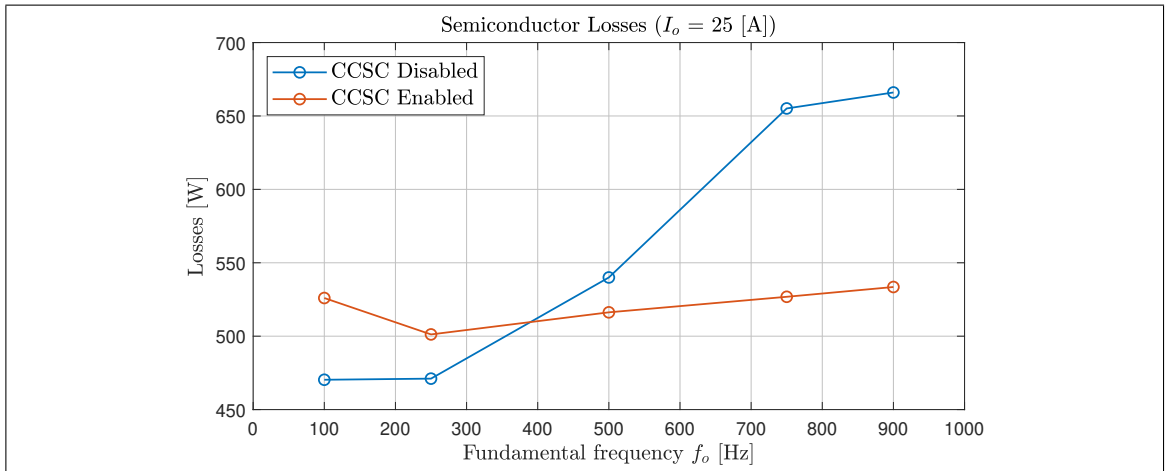


Figure 5.9. ALE-MMC Losses at different fundamental frequencies.

5.6. Comparison with Two-Level Inverter

The two-level inverter is a classic and standard solution for variable speed drives due to its simple structure and control. Only six semi-conductor devices are needed, and as there are no energy storage passive components (capacitor or inductors), its primary control loop

involves only the output current control. Thus, it is of interest to compare the performance of ALE-MMC with a Two-Level inverter in similar conditions.

The same thermal model for the 100 V, 300 A IPT020N10N3 Infineon MOSFET is used for the ALE-MMC, while a thermal model of the 600 V, 109 A IPW60R017C7 Infineon MOSFET is implemented for the Two-Level inverter. The switching frequency of the Two-Level inverter is set to 10 kHz. The parameters for the ALE-MMC are the same shown in Table 5.1, except for the SMs switching frequency, which is reduced to 1 kHz in order to have a similar equivalent switching frequency with the Two-Level inverter. The load is the same as in Table 5.1 for both converters.

The results for both converters driving 5.6 kW at $f_0 = 50$ Hz are shown in Figure 5.10, with the relevant waveforms and losses in one fundamental cycle. As can be seen, the output current THD in the Two-Level inverter is six times greater than in the ALE-MMC. The ALE-MMC has less ripple on the output current due to the modular property of the converter, which allows smaller steps on the output voltage, and thus less voltage applied to the inductor in the transitions.

The estimations also show that the ALE-MMC has lower semi-conductor losses even when it has a considerable higher number of devices. The ALE-MMC devices operate at a tenth of the DC-link voltage, while the Two-Level inverter devices must withstand the full DC-link voltage. Thus, the switching losses on the Two-Level inverter will be higher on each device. On the other hand, the on-state resistance of the ALE-MMC MOSFETs are lower, and so are the conduction losses. The combined effect of lower on-state resistance plus the lower voltage stress on the devices makes the semi-conductor losses on the ALE-MMC lower than the Two-Level inverter in this case.

It must be considered that the losses on the Two-Level inverter are concentrated on only six devices, while in the ALE-MMC are distributed between 360 devices (or 30 modules). So the Two-Level inverter may be considerable smaller and less complex than

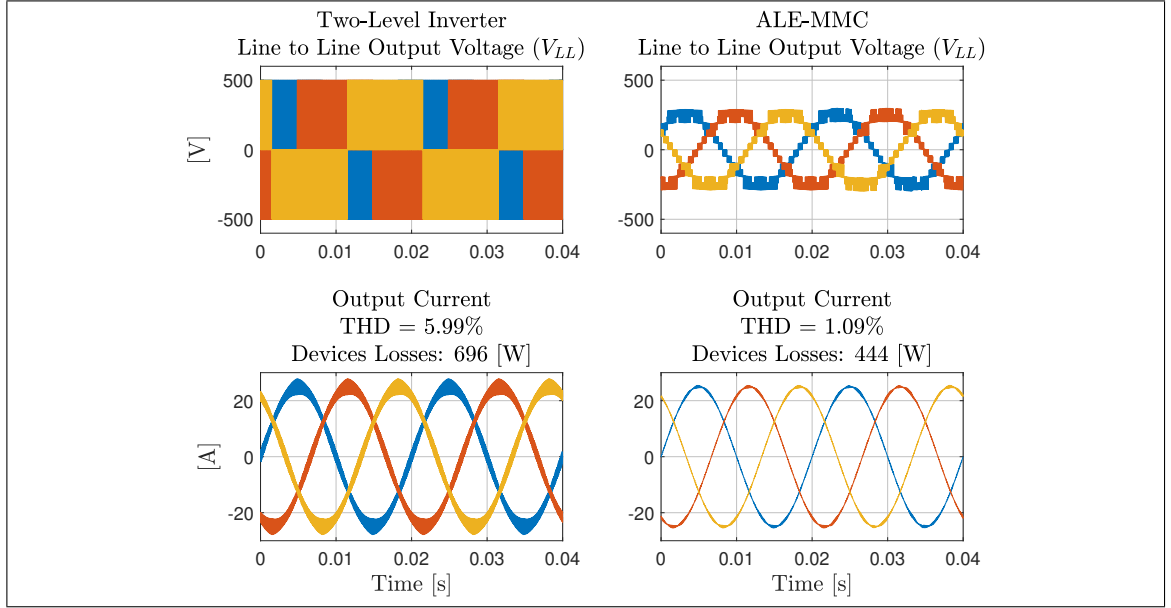


Figure 5.10. Comparison between Two-Level Inverter and ALE-MMC - $I_o = 25$ A, $f_0 = 50$ Hz.

the ALE-MMC, but the cooling system of the latter may be considerable simpler, which is an important factor to consider.

Finally, the initial estimation shows that the ALE-MMC will have less semi-conductor losses and THD compared to a MOSFET Two-Level inverter in similar conditions. Even when the switching frequency of the ALE-MMC SMs is increased to 10 kHz, the losses are still comparable to the Two-Level inverter, as can be inferred from Figure 5.9. However, this comparison does not consider the transformer core losses of the DABs. In order to compare efficiencies, a detailed thermal model of the DAB transformer must be developed to estimate its losses under these conditions, which is out of the scope of this work.

6. EXPERIMENTAL RESULTS

A small scale single-phase ALE-MMC prototype was developed for experimental validation for both theory and simulation results. Figure 6.1 shows the ALE-MMC and the new modules. Each module is composed by the classical SM with its capacitor plus one of the H-Bridges of the DAB. Then, a HF transformer with 1:1 ratio is used to link an upper and lower module, forming the coupled system. Only ceramic capacitors were used in the SMs without any electrolytic type. The upper Printed Circuit Board (PCB) contains the respective gate drivers for both SM Half-Bridge and DAB H-Bridge, while the lower PCB contains all the power circuitry and semi-conductor devices. The OptiMOS™ IPT020N10N3 MOSFETs, whose the thermal model was developed previously, were used for both SM and DAB.

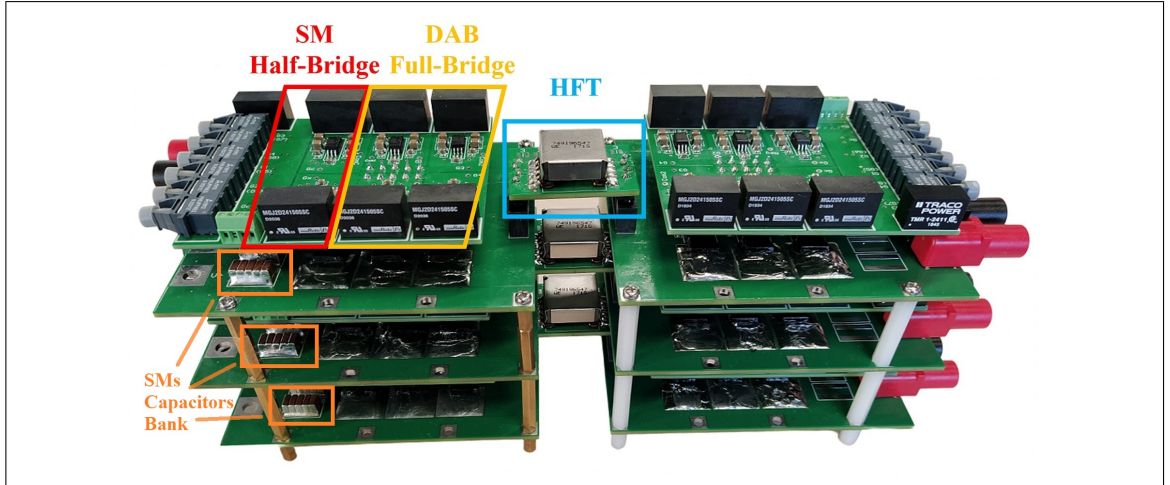


Figure 6.1. Single-phase ALE-MMC experimental prototype. Upper and at the left, and lower at the right. Both with $N_{SM} = 3$ SMs.

The modules are intended to operate with the parameters shown in Table 6.1. The load resistance, the DC-link voltage and thus the SM mean voltage will vary depending on the experiment and they will be indicated in each test. As the MOSFET are rated for 100 V, the SM voltage will vary between 40 and 70V in order to maintain a safe margin. Finally, with these parameters, the circulating current resonance average frequency is 678.14 Hz,

which will occur when $f_0 = 339.07$ Hz approx. Nevertheless, this may vary due to the parasitic effects of the involved components.

Table 6.1. Experimental parameters.

Variable	Symbol	Value
Number of Cells per Arm	N_{SM}	4 [-]
Sub-Module Capacitance	C_{SM}	270 [μ F]
DAB Total Inductance	L_s	1.6 [μ H]
Arm Inductance	L_{arm}	204 [μ H]
Load Inductance	L_{Load}	2 [mH]
Load Resistance (if not specified)	R_{Load}	11 [Ω]
Half-Bridge switching frequency	$f_{sw,MMC}$	10 [kHz]
DAB switching frequency	$f_{sw,DAB}$	100 [kHz]

Considering the single-phase converter, a DC-link mid-point was implemented by using capacitors in order to connect the load to it. This may have an effect on some experiments since these capacitors may absorb enough charge in some tests and affect other converter variables. In a three-phase converter these effects are not expected since there is no need to use a DC-link mid-point in most cases.

6.1. Operation with DABs disabled

Before entering into the standard operation, it is of interest to compare the ALE-MMC operation with the DABs function disabled. Figure 6.2 shows the ALE-MMC operating with all the DABs H-Bridges disabled, so only the SMs are being used, where V_{SM}^{avg} is the ideal SM voltage ($\frac{V_{DC}}{N_{SM}}$). i_u , i_l , i_o and i_z are the upper, lower, output and circulating currents, respectively, while $v_{SMj,u}$ $v_{SMj,l}$ are the upper and lower voltages of the j -th SM, respectively.

As can be seen, the converter is driving an output current of around 1 A, and with the DABs disabled it is an enough current to increase the SM voltage up to 33% of the target value (20 V over the mean value of 40 V). Also, the voltages start deviating from its DC value. The oscillations are increased because of the low capacitance used in the SMs (270

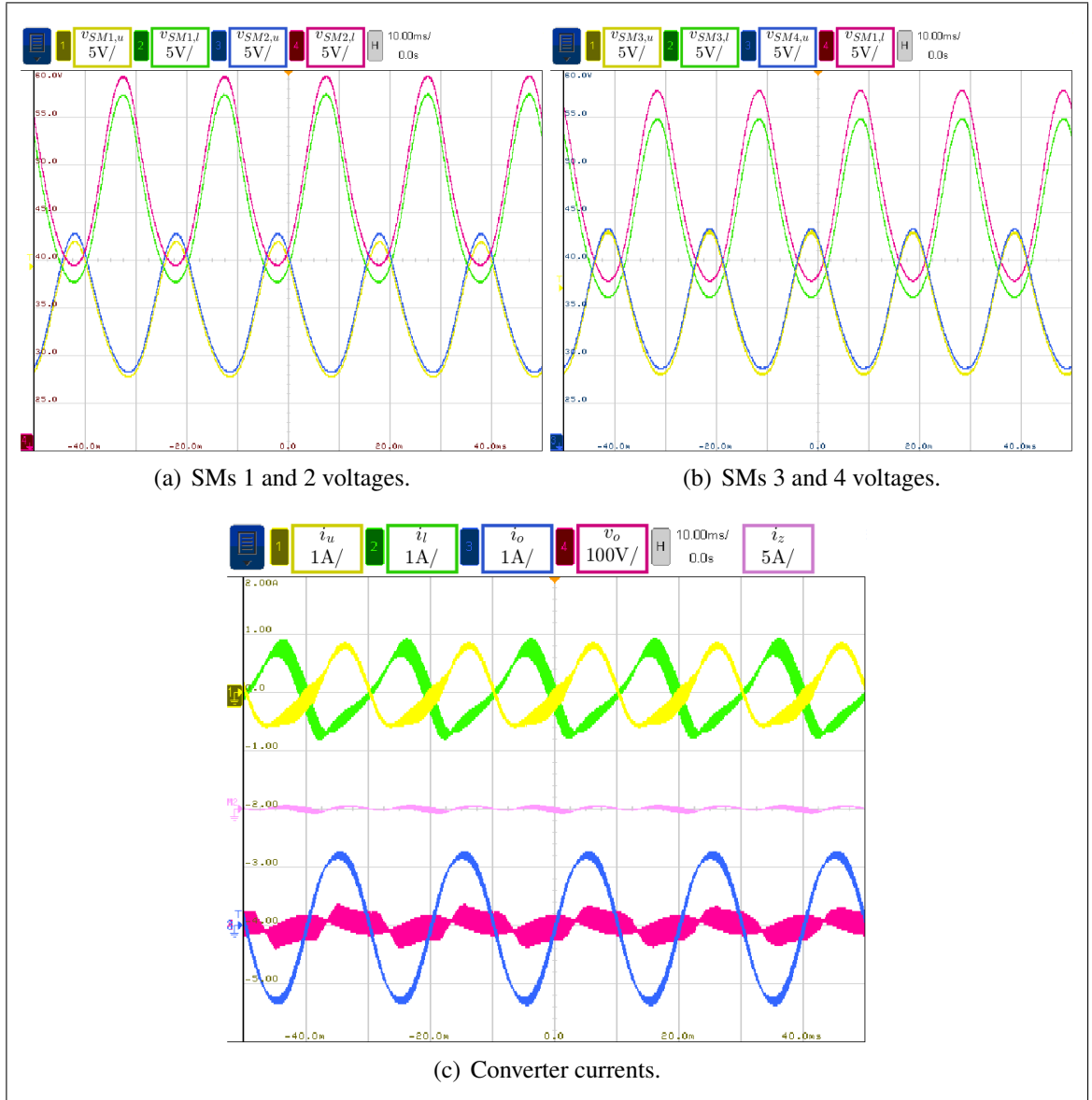


Figure 6.2. ALE-MMC operation without DABs. $V_{SM}^{avg} = 40$ V, $f_0 = 50$ Hz.

μF). And even if no balancing algorithm is implemented in the experiment, it would not reduce significantly the voltage ripple.

Figure 6.3 shows the normal operation with the DABs active. In this case, the converter is driving an output current of 8 A and the oscillations are 1 V approx. These results shows the effectiveness of the incorporation of the DAB for reducing the voltage oscillations, even with a small SM capacitance of 270 μF . Therefore, the working principle of the

ALE-MMC is validated with this prototype. The small harmonics present on the SMs voltages are mainly due to the dead-time being used for both SMs and DAB.

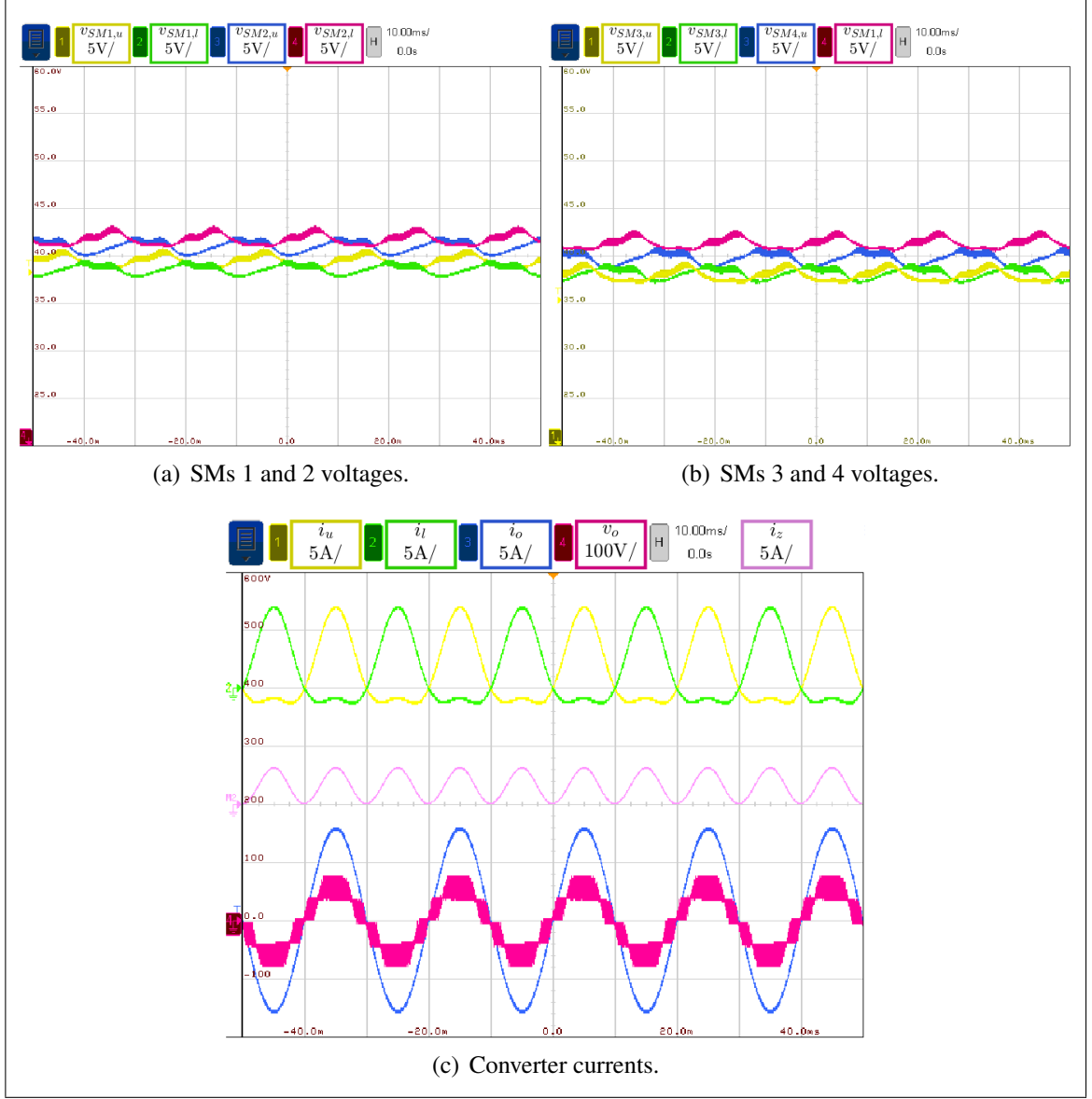


Figure 6.3. ALE-MMC normal operation with DABs. $V_{SM}^{avg} = 40$ V, $f_0 = 50$ Hz.

Given that the coupled SMs behavior are basically the same for each couple pair, from now only the waveforms for SM 1 and SM 2 will be shown. SMs 3 and 4 will have basically the same shape, as can be inferred from Figures 6.2 and 6.3.

6.2. Standard Operation

The following experiments shows the ALE-MMC operating with the basic control loops at different frequencies. For the SMs voltages oscilloscopes, DC offsets are used to differentiate the coupled SMs, but it must be considered that all of them are around their target voltage approximately.

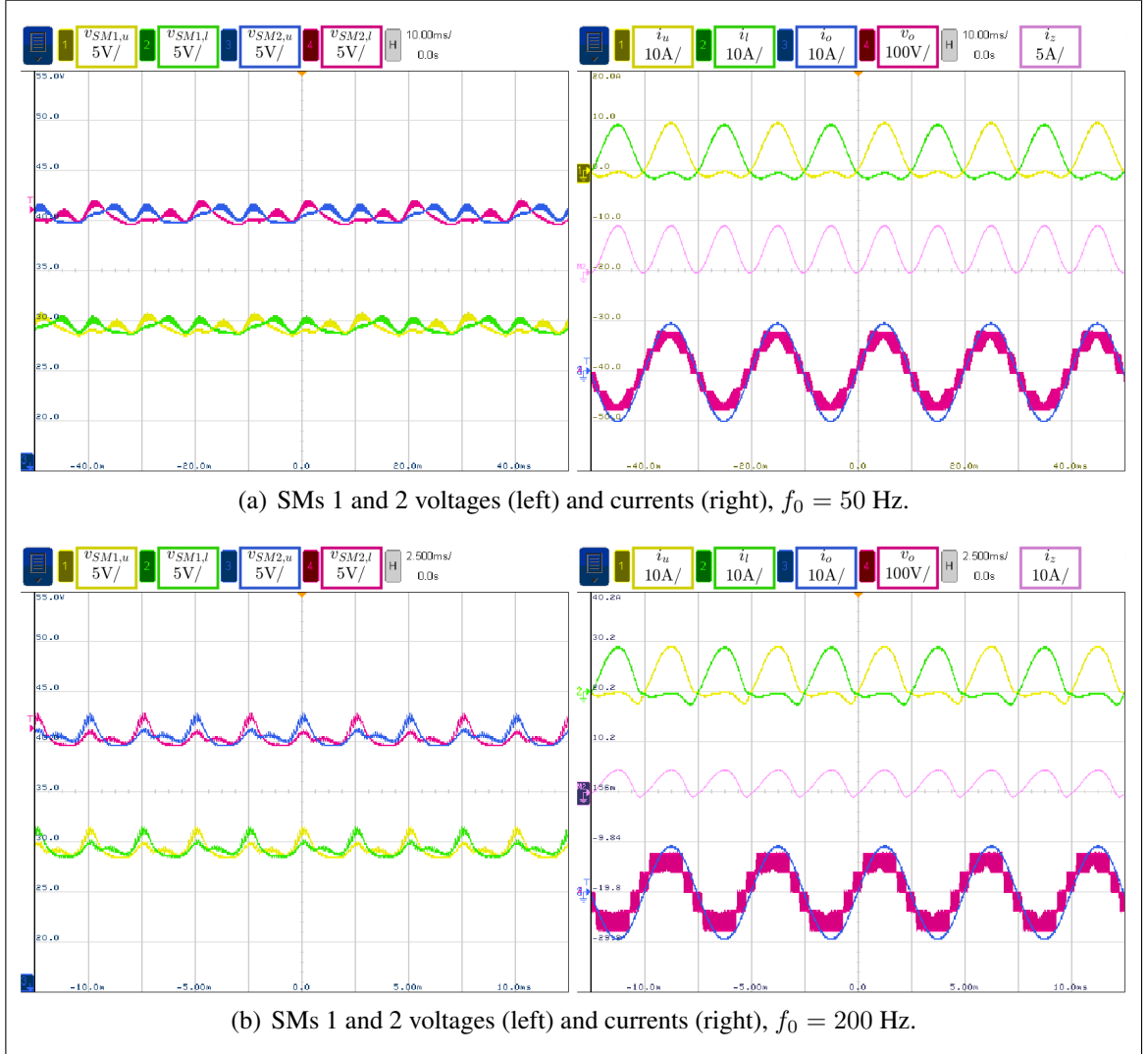


Figure 6.4. ALE-MMC operation at 50 and 200 Hz. $R_{Load} = 7.3 \Omega$, $V_{SM} = 40$ V, $m_o = 1$.

Figure 6.4 shows the operation of the converter at 50 and 200 Hz, with maximum modulation index, while Figure 6.5 shows the operation for 500 and 700 Hz.

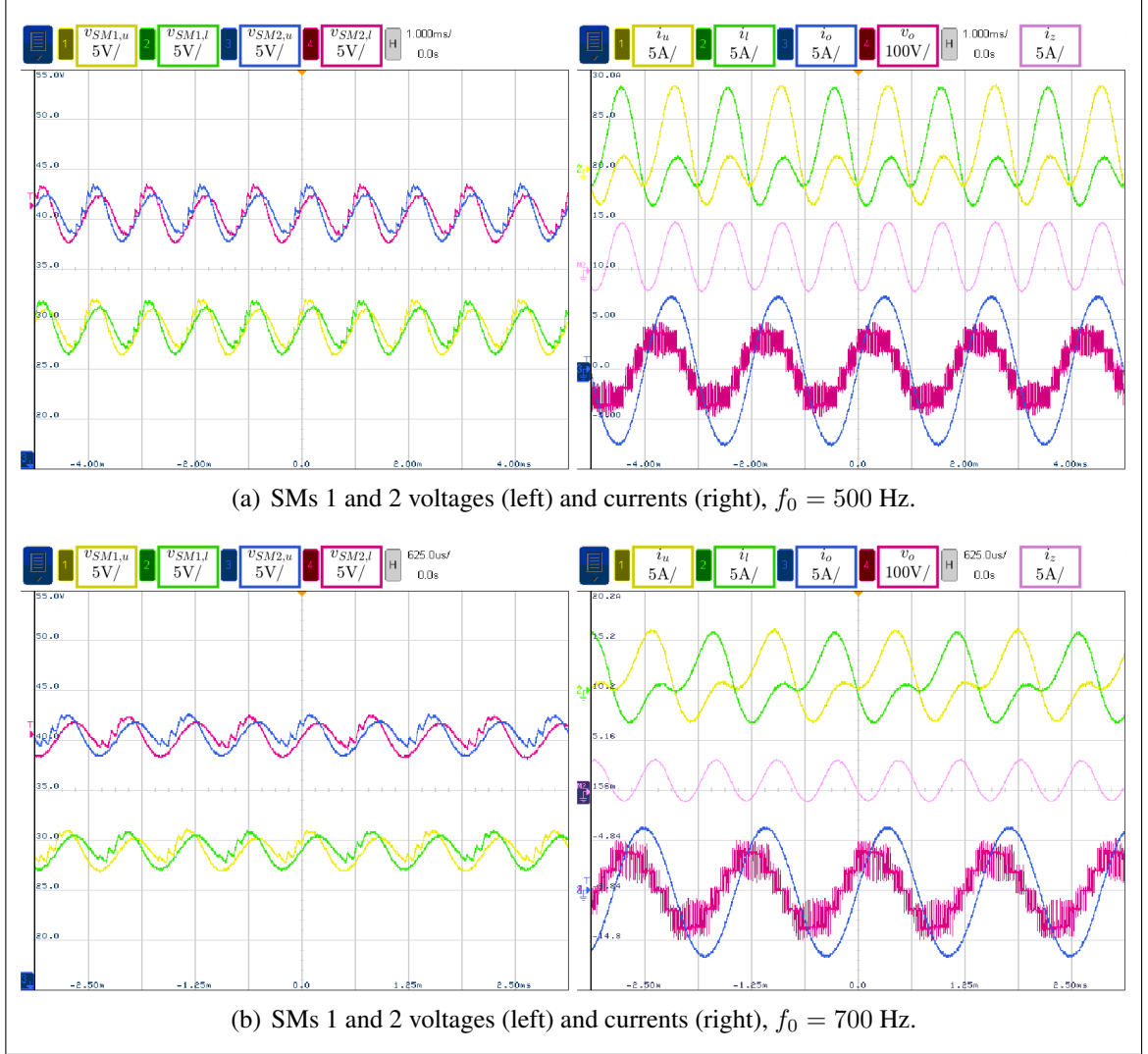


Figure 6.5. ALE-MMC operation at 500 and 700 Hz. $R_{Load} = 7.3 \Omega$, $V_{SM} = 40$ V, $m_o = 1$.

Results from Figures 6.4 and 6.5 shows a proper behavior for the ALE-MMC prototype, where all the results are similar to the ones in the simulations. At low frequencies (50 and 200 Hz), the voltage is well maintained at the DC value while driving an output current of 10 A approx. There are small harmonics present in the voltage

waveforms, but these are mainly due to the deadtime implemented in the converter. The experiments carried out maintained a relative high deadtime due to safe and hardware issues, with a value of $1\text{ }\mu\text{s}$ for the SM Half-Bridges, and 500 ns for the H-Bridges, but they can easily be reduced. If reduced, the voltage waveforms will be similar to the ones of the simulations. The output current has a proper sinusoidal waveform while the output voltage clearly shows the voltage steps thanks to the low voltage ripple.

For higher frequencies, it can be seen how the harmonic content of the arm currents change due to the angle shifts and the circulating current. Also, it can be seen at 500 Hz (Figure 6.5(a)), which is closer to the critical frequency where the resonance is produced (339.07 Hz), i_z is higher than in the 700 Hz case, even when the current is almost the same. This is reflected in the SMs voltage, which exhibit a higher amplitude compared to the other cases. However, the DAB maintains both coupled capacitors practically at the same voltage. In all cases, the output current has a proper form and the SMs volages maintain a low ripple.

Some consideration must be taken at lower frequencies due to the DC-link capacitors mid-point implemented. As these capacitors do charge and discharge depending on the output current (and frequency), then these oscillations are reflected on other variables of the converter. To this, other components parasitic effects are involved and added to this effect. Figure 6.6 shows the operation of the ALE-MMC at 10 Hz driving 5 A of output current. The SMs voltage present a fundamental frequency oscillation because of the effects mentioned before, but the DABs still maintain the coupled capacitors at the same level. The oscillations are at a good level with an amplitude of 2.5 V approx above the nominal value. The output current has a sinusoidal form and and no distortion or harmonics are seen. In this data, the output voltage v_o is not representative due to the large time window being used, where the sampling and filtering effects distorts the original waveform with the switching behavior.

Summarizing, the same effects expected from the simulation are replicated in the real converter except for the low frequency behavior. However, the differences between the

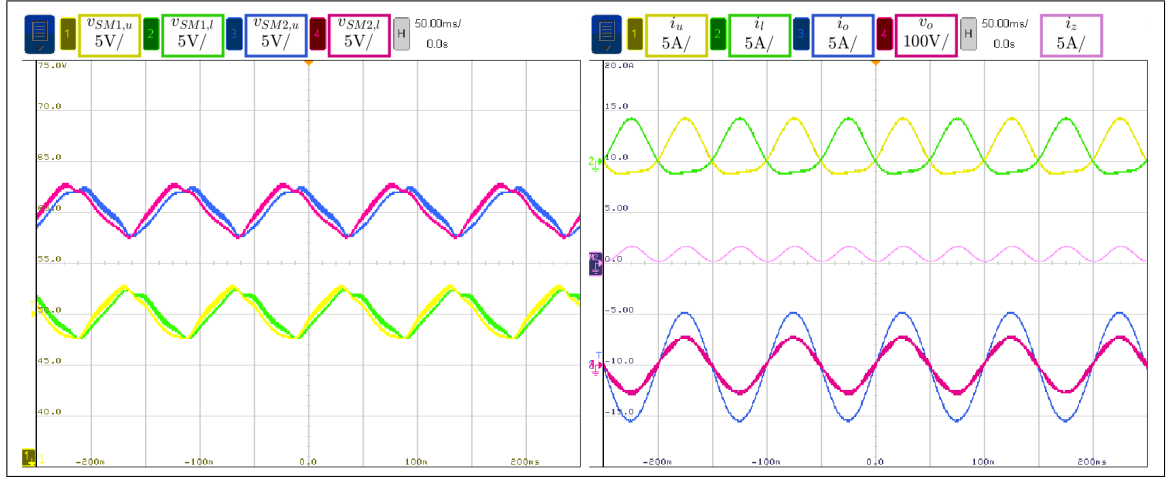


Figure 6.6. ALE-MMC operation at 10 Hz. $R_{Load} = 10 \Omega$, $V_{SM} = 50 \text{ V}$, $I_o \approx 5 \text{ A}$.

simulation and experimental results at lower frequencies are explained by the circuitry differences between a single and a three-phase converter, but also due to parasitic effects and preventive measures such as deadtimes. Thus, the theoretical analysis made is validated with these experiments, and the basic function and operation of the ALE-MMC is verified experimentally.

It would be desirable to include an experiment for the DC output current scenario. However, the fact of using capacitors for the DC-link mid-point prevents this experiment from being performed. When a DC output current is driven, one of the DC-link capacitors is constantly charging while the other is discharging. This causes the output current to decrease accordingly until it becomes zero. Thus, it is not possible to continuously perform this test. This issue could be solved by using two DC voltage sources in series, but it was not possible due to laboratory limitations. Nevertheless, the previous simulations and the similarity of the simulations with the experimental tests are enough to predict that the converter will be capable of handling DC currents given the conditions. In a three-phase converter, as there is no need for DC-link mid-point, it is possible to perform the DC output current test.

6.3. Circulating Current Suppression

With the standard operation verified, now the experiments suppressing the circulating current are shown. The voltages of SM 3 and 4 are still omitted since they have the same behavior as SMs 1 and 2.

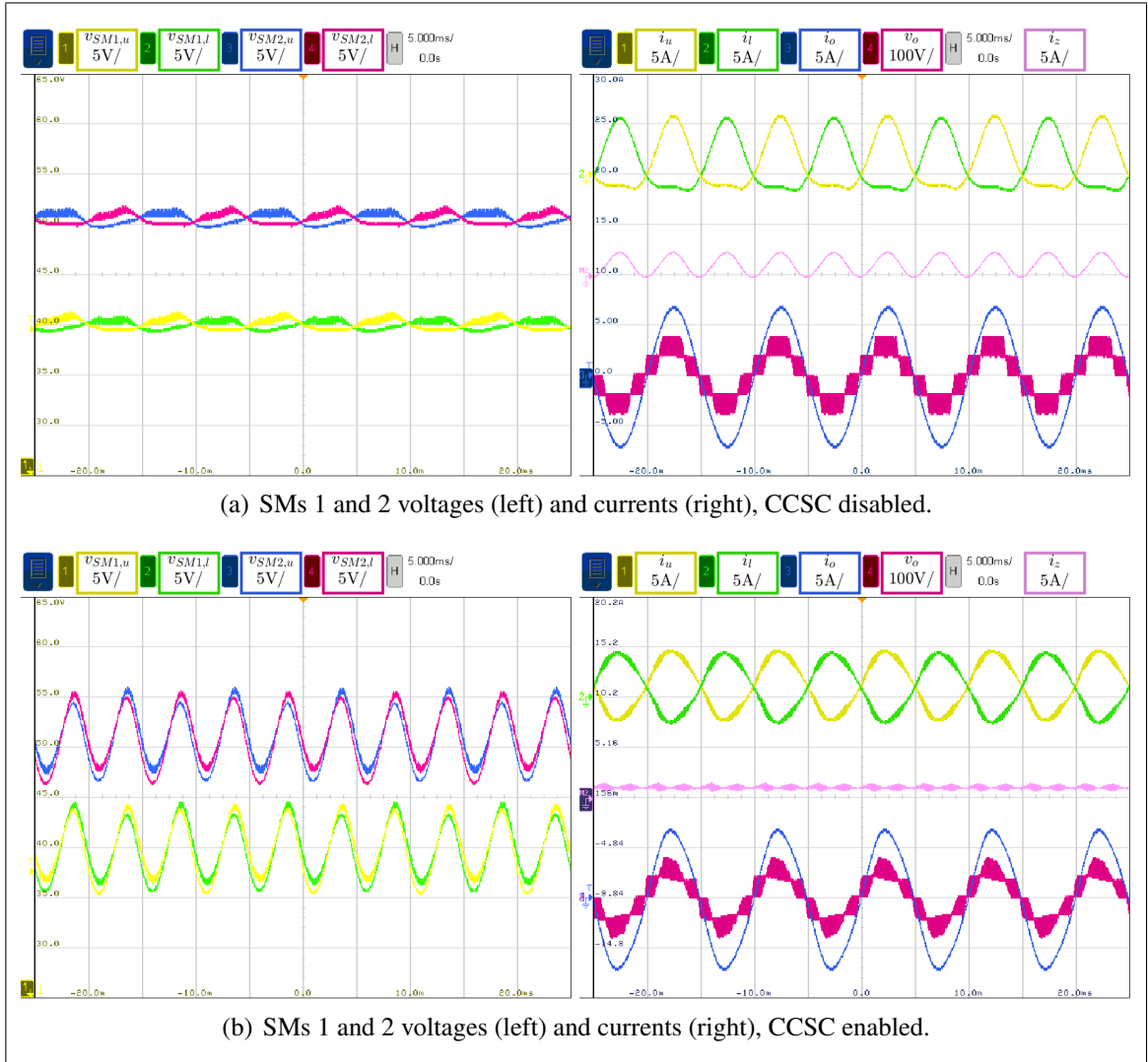


Figure 6.7. CCSC operation at 100 Hz. $V_{SM} = 40$ V, $I_o = 7$ A.

Figure 6.7 shows the results with and without CCSC at 100 Hz. The results show the same behavior obtained from the simulation in Figure 5.4(a). Before enabling the CCSC,

the SMs voltages are well maintained at their DC value with minimal ripple. When the CCSC is enabled, the voltage ripple increases considerably, and the circulating current is not well maintained at its DC level, both effects that were expected from the theoretical analysis and the simulation results. The circulating current helped together with the DAB to maintain a low voltage ripple on the SMs, so its elimination at low frequencies causes the voltage oscillations to increase. The output current is also affected and distorted, but this is a consequence of the low number of SMs (N_{SM}) being used, where the ripple and different effects have more influence on the other variables. In the simulation of Figure 5.4(a), the output current is practically not affected after enabling the CCSC, even with higher voltage ripple.

Figure 6.8 shows the experimental results for the CCSC operation at 500 Hz. Without CCSC the circulating current AC component is relatively high since the converter is close to the critical frequency, and the effect is notorious on the arm currents. The SMs voltages have oscillations at twice the fundamental frequency, and the DAB keeps both coupled voltages equal. After enabling the CCSC, the circulating current is set effectively to its DC value, and the arm currents have only the DC component and the fundamental frequency component, so their RMS value is reduced. The SMs voltage ripple are slightly reduced after enabling the suppression, so their maximum value is also reduced. The more the output current, the greater the effect of suppressing the circulating current. All these results were expected from the theoretical analysis, and are practically the same from those of Figure 5.4(b).

Figure 6.9 shows the results for the CCSC operation at 700 Hz. The behavior with and without CCSC is similar to the 500 Hz case, but the reduction of the SMs voltage ripple is more noticeable. This can be explained by the fact that the DAB greatly improves its performance when its third harmonic is eliminated thanks to the CCSC. In this case, an harmonic of 2100 Hz in the DAB current and the transformer is suppressed, leaving only the fundamental frequency harmonic on them. As the DAB acts as low-pass filter, it is easier for it to transfer low frequency harmonics.

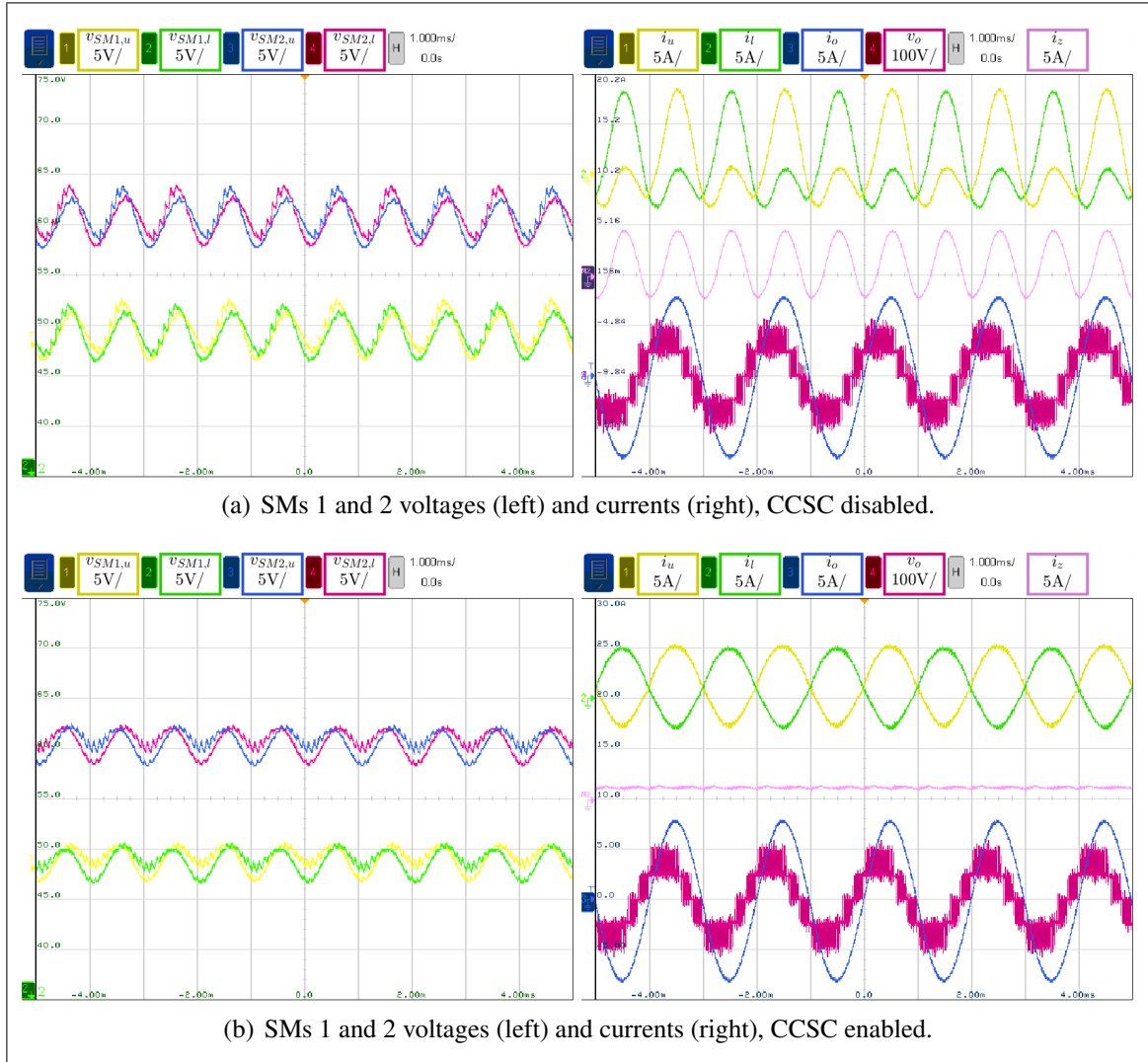


Figure 6.8. CCSC operation at 500 Hz. $V_{SM} = 50$ V, $I_o = 8$ A.

Summarizing, the CCSC operation and effects at different frequencies was tested, and the results were as expected from both the analysis and the simulations. At low frequencies, the CCSC increases the voltage ripple and lowers the ALE-MMC performance. On the other hand, at higher frequencies the CCSC improves the converter performance and its variables, lowering the SMs voltage ripple and easing the DAB power transfer. Thus, the proposed logic for enabling the CCSC allows to solve the high frequency issues regarding this topology.

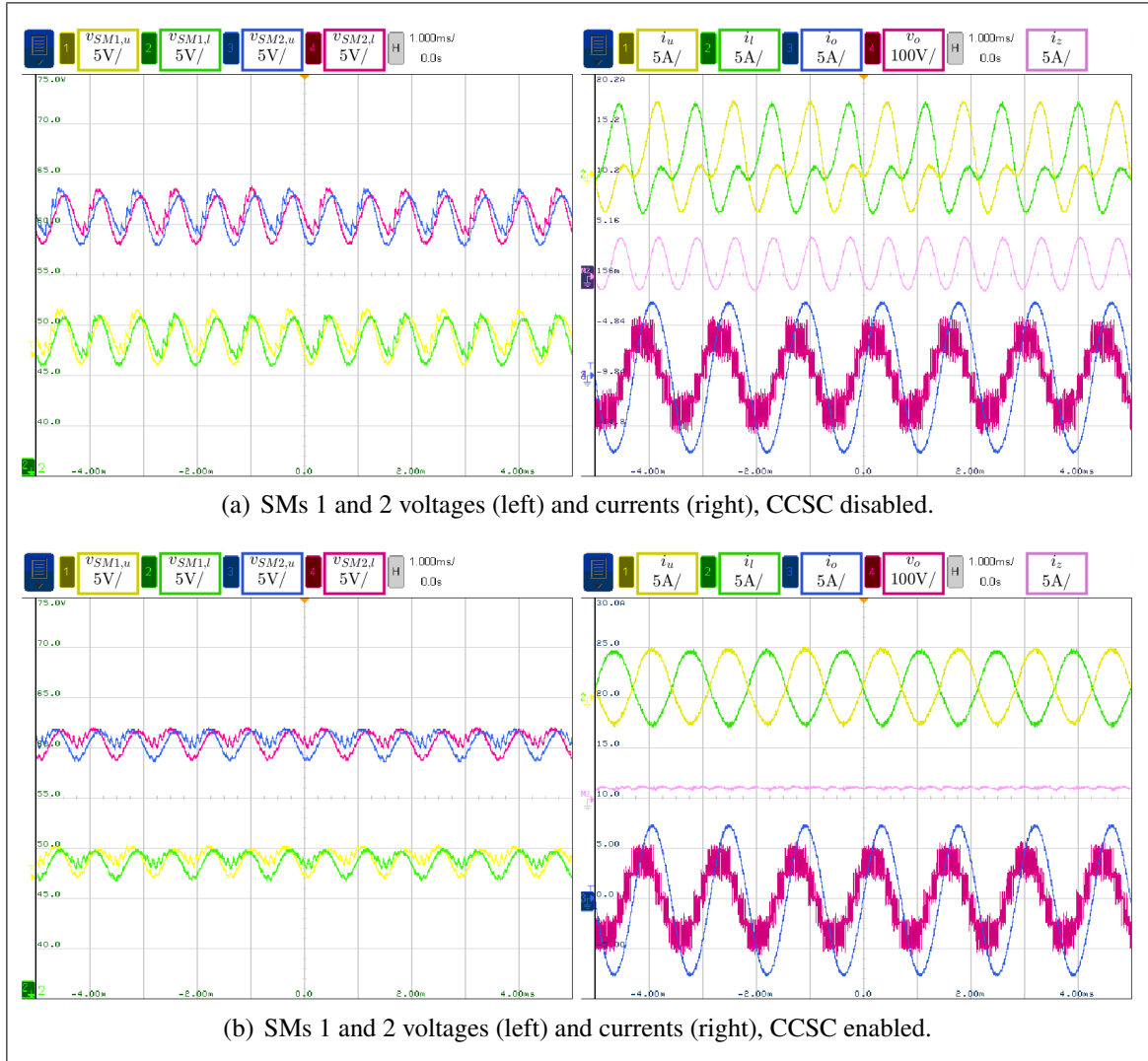


Figure 6.9. CCSC operation at 700 Hz. $V_{SM} = 50$ V, $I_o = 7.5$ A.

Another important aspect to consider is the efficiency variation with and without CCSC. For this, the converter information given by the power analyzer is compared before and after enabling it. Figure 6.10 shows the converter information at different frequencies, with and without CCSC, where η_1 is the efficiency measured between input and output power. The information shows that enabling the CCSC at low frequency (100 Hz) reduces the efficiency of the converter, in this case by 0.535 %. This can be explained by the fact that the voltage ripple in this case increases, so the switching losses of the SMs and

H-Bridges increases too. The reduction of conduction losses does not compensate the increase of the switching losses, so the efficiency decreases.

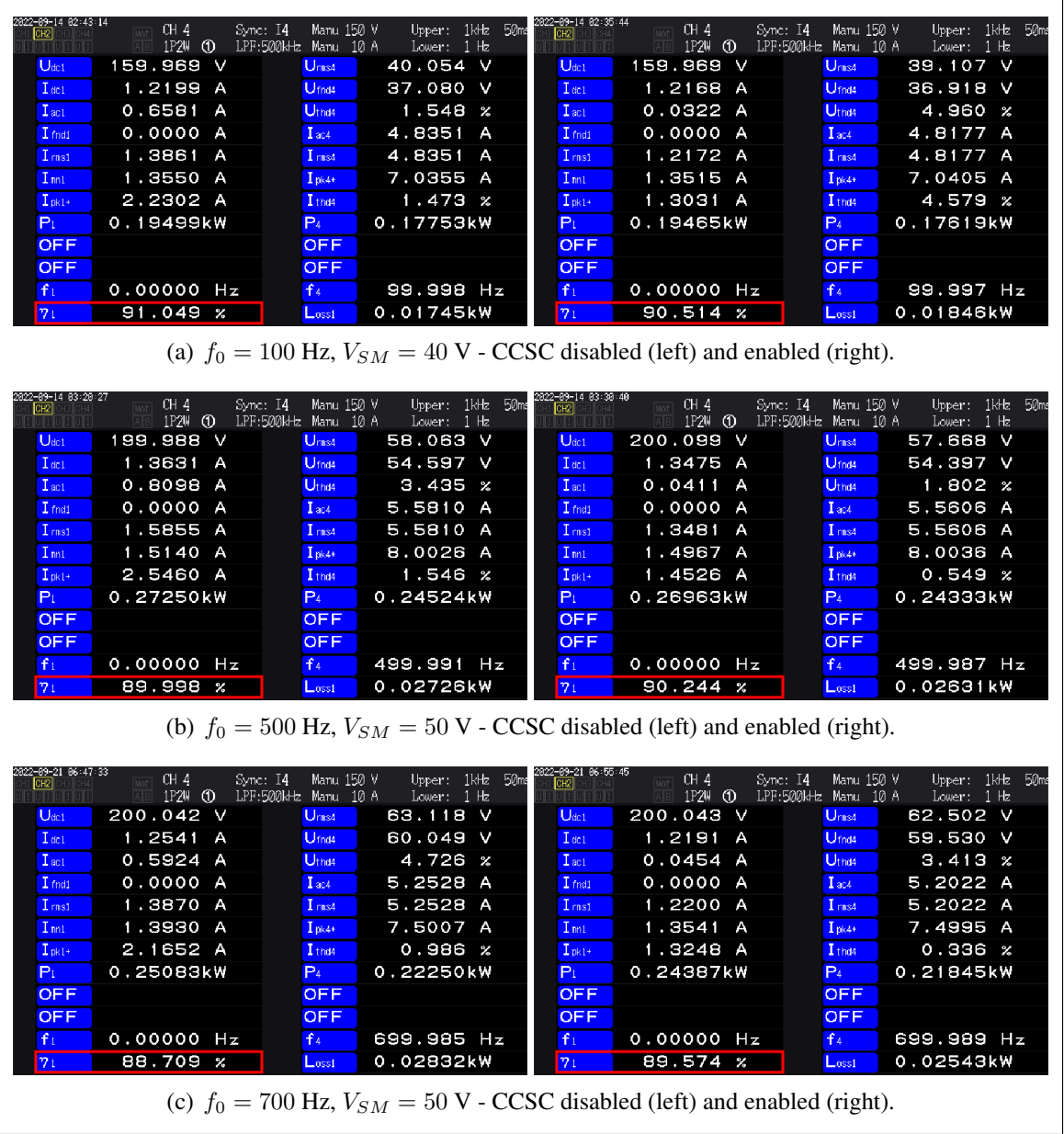


Figure 6.10. ALE-MMC power information with and without CCSC enabled.

At higher frequencies, the CCSC increases the efficiency by 0.226% for the 500 Hz case, and by 0.865% for the 700 Hz case. Part of this increase in efficiency is due to

the reduction of the SMs voltage ripple and also the elimination of a third harmonic in the DAB transformer. The other factor is the reduction of the conduction losses, since the AC circulating current has a higher amplitude in this range. Thus, the overall effect is an increase in the efficiency of the converter at high frequencies. Another relevant aspect of the CCSC in this range is that it decreases the THD of the output current, as the I_{thd4} variable in Figure 6.10 shows. For the 500 Hz case it is reduced by a 0.997%, and for the 700 Hz it is reduced by a 0.65%. As there is a lower voltage ripple and the second harmonic current was suppressed, their effects are less on the output current, and thus decreases the THD. Consequently, the power quality increases in this range when the suppression is enabled.

These results regarding the losses and efficiency of the converter are coherent with the losses estimation made in Figure 5.9 with and without CCSC. Here, the case with lower losses at low frequency occurs with the CCSC disabled, and at higher frequencies occurs with the CCSC enabled, similar to the behavior of the CCSC experiments. Thus, the simulation estimation is validated with the experimental prototype. However, it must be considered that the prototype is a single-phase for low power scale. Due to laboratory limitations, it was not possible to obtain higher output power in order to have a better representation of the system. However, with higher power the overall efficiency increases (as further results will show), and consequently the effects of the CCSC will be higher. Therefore, the same behavior is expected for a higher power converter up to certain point, matching losses behavior of the simulations and the experiments.

A transition after enabling the CCSC at 500 Hz is shown in Figure 6.11 for observing with better details the transitions and changes of the different variables. While the circulating current approaches its DC value, the arm currents decrease their amplitude and start to have only a fundamental frequency component (plus the DC term). Also, it is easier to compare the voltage ripple before and after the CCSC. The SMs voltage ripple is slightly decreased in this case, but if the output current or the fundamental frequency were higher, the effect would be more notorious, as Figure 6.9(b) shows.

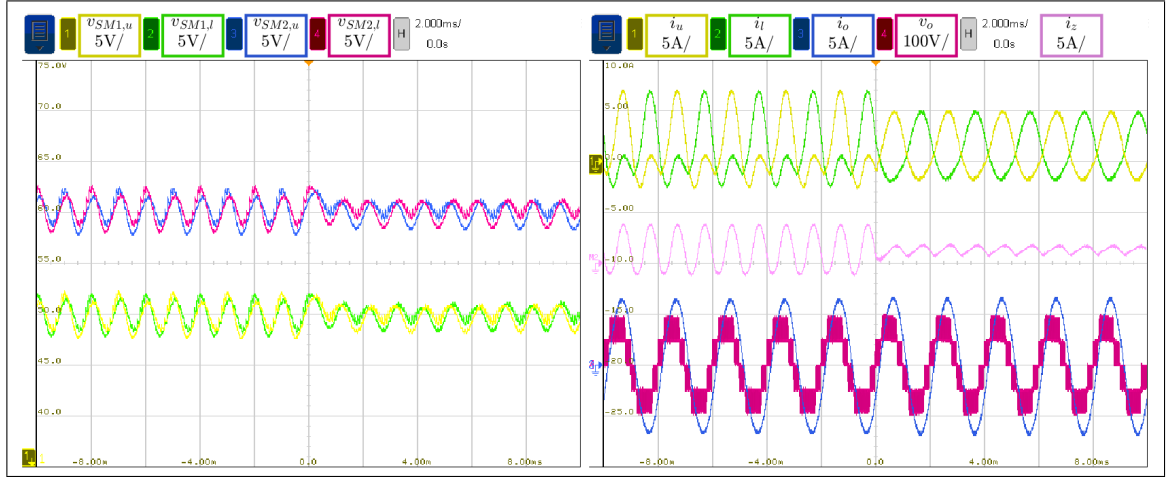


Figure 6.11. CCSC transient at 500 Hz, SMs voltages (left) and currents (right). $V_{SM} = 50$ V, $I_o = 6.8$ A.

6.4. Frequency Transients

With the steady-state experiments done, the ALE-MMC must be tested in variable frequency conditions to evaluate its performance and behavior.

Figure 6.12 shows a transition from 200 to 700 Hz in 50 ms, with a constant current of $I_o = 5.8$ A. The main purpose of this test is to show the circulating current resonance range in the converter. As can be seen, there is a time range where the circulating current increases in amplitude, which corresponds to the critical frequencies where the resonant frequency oscillates. The effect of this circulating current rise is clearly seen in both the arm currents and the SMs voltages. After this range, the circulating current starts to decrease its AC amplitude.

In the frequency ramp simulation from Figure 5.3, the effects of the circulating current resonance were extremes due to the idealities of the converter. But in the real converter the effects of the resonance are not as extreme as in the simulation, as the actual test shows. In this case, a relatively low current is being driven, but if a higher power is driven by the converter then the effects of the resonance also increase.

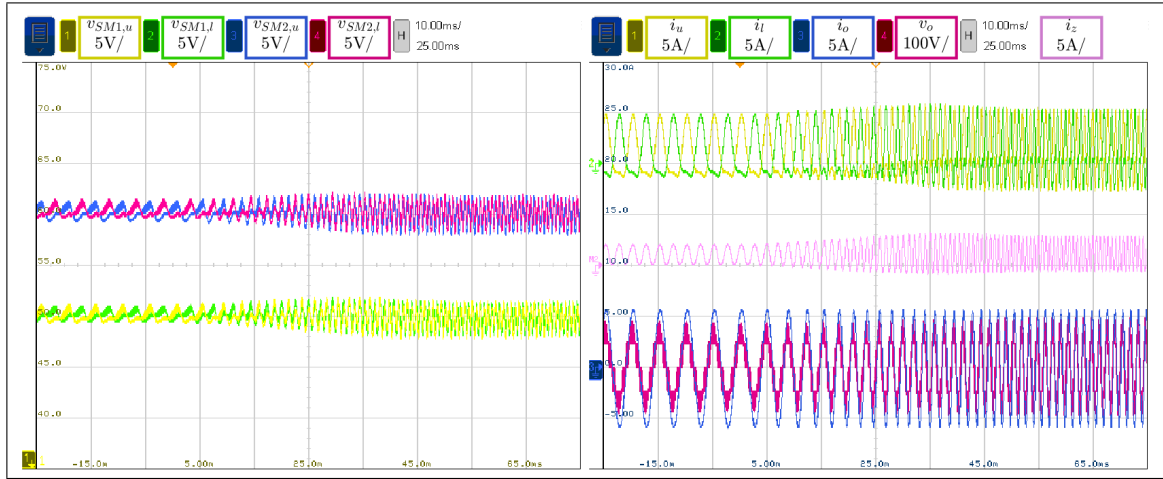


Figure 6.12. Frequency transient from 200 to 700 Hz in 50 ms, SMs voltages (left) and currents (right). $V_{SM} = 50$ V, $I_o = 5.8$ A.

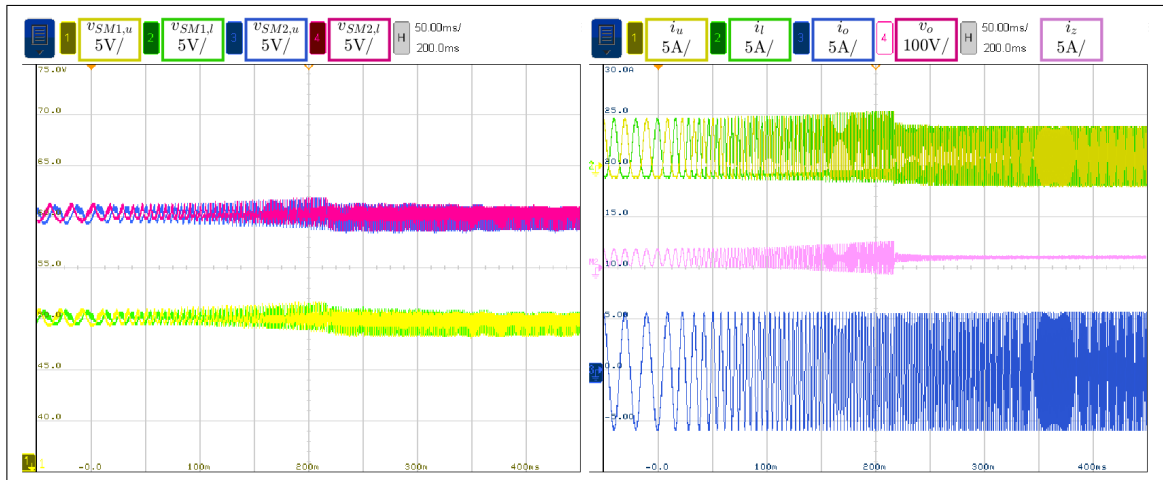


Figure 6.13. Frequency transient from 50 to 700 Hz in 400 ms, SMs voltages (left) and currents (right). $V_{SM} = 50$ V, $I_o = 5.8$ A.

Figure 6.13 shows a wider frequency ramp transient from 50 to 700 Hz in 400 ms, where the CCSC is enabled after reaching 400 Hz. As expected, the suppression of the circulating current decreases the arm currents amplitude and its RMS value, and also helps the SMs voltages to have a lower voltage ripple. This is proven by comparing the amplitudes of the different variables in Figures 6.12 and 6.13. As mentioned before, the benefits of enabling the CCSC are greater as the output power of the converter increases,

so with a higher power ALE-MMC prototype, the efficiency increase and the improvement of the waveforms will be more valuable.

6.5. Efficiency Curves

The ALE-MMC operation was verified in different scenarios with all the previous tests, giving good results and proving the theory and simulations. Given this, it is important to have an initial analysis about the efficiency and overall performance of the converter.

It must be considered that this low scale ALE-MMC prototype was built mostly for operation verification purposes, and given different laboratory limitations, it was not possible to recreate full power scenarios (neither three-phase operation). However, the information given by the power analyzer give a good insight of the overall performance of the converter, and could be scaled to higher powers.

Figure 6.14 shows the converter prototype operating at 1.1 kW approximately, a relative high power compared to the maximum supported by the limitations (mainly current limitations). In order to obtain these waveforms the test was performed for a short period of time. The SMs mean voltage was increased to 70 V, which is equivalent to use a 280 V DC-link. This, in order to increase a higher achievable current given the load and have a better start point to analyze the power. The SMs voltages have a ripple of 2.5 V approximately (3.5% of the DC value), even while driving an output current of 17 A with a SM capacitance of 270 μ F.

The overall efficiency of the converter in these conditions is 94.062%, however, some observations must be made before drawing conclusions. The first point is that this converter was built for operation verification purposes, and some components have current limitations that prevent reaching powers greater than those of Figure 6.14. The second observations is that the dead-time is relatively high due to the hardware used. However, this can be easily reduced and it would improve both efficiency and the SMs waveforms.

Third, an important factor to consider is that no cooling system was implemented in these tests. Although the losses are relatively low compared to the semi-conductor ratings, still their temperature is not controlled. Finally, the converter would improve its efficiency if more power was handled, at least until a cooling system is needed for proper operating conditions.

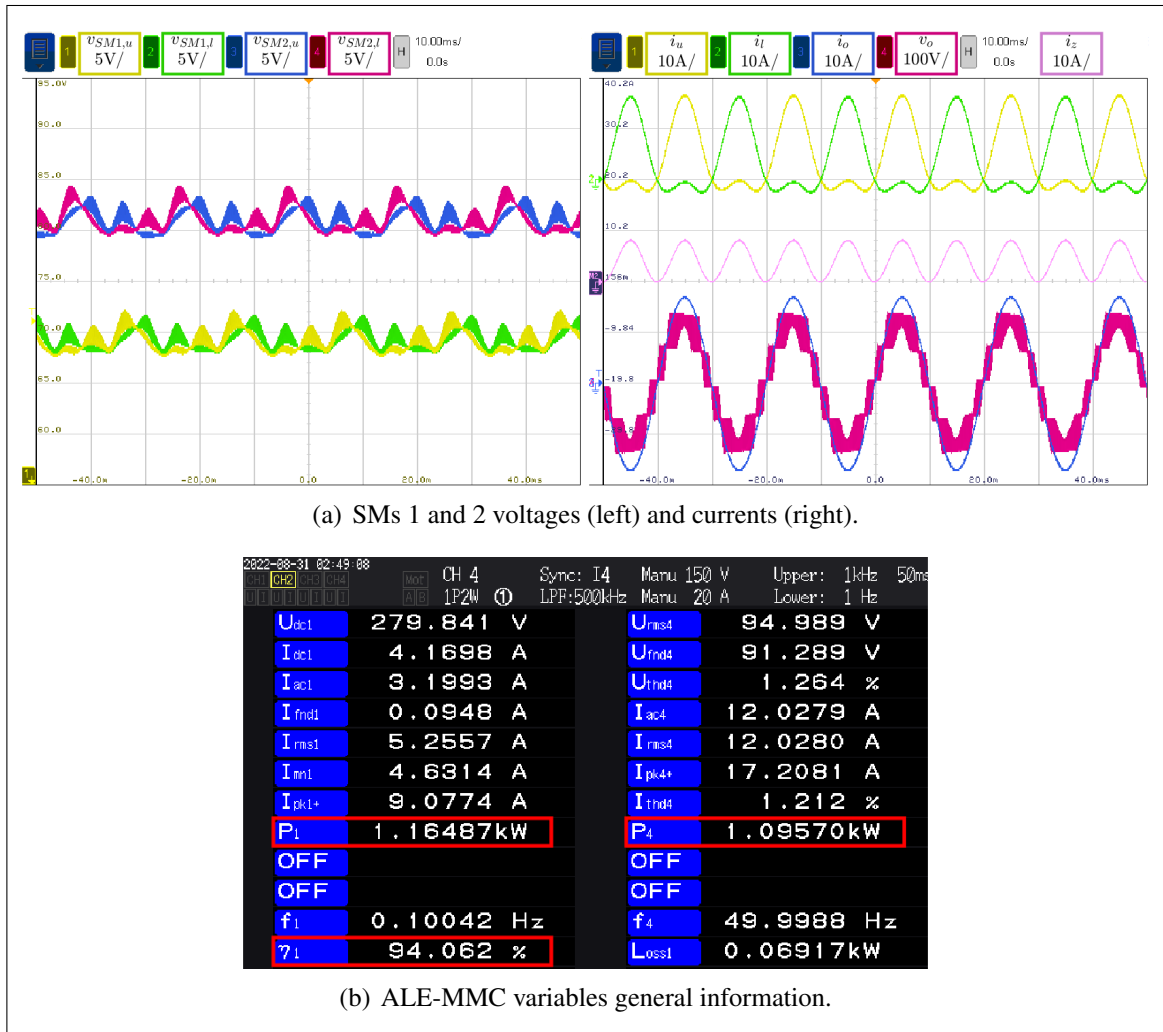


Figure 6.14. ALE-MMC operation at 1.1 kW approximately. $V_{SM} = 70$ V, $I_o = 17$ A, $\hat{n}_o = 1$, $R_{Load} = 7.3 \Omega$.

To prove and give insights about the above, efficiency curves are obtained experimentally for different conditions. Figure 6.15 shows the efficiency as function of

the modulation index for different output frequencies. As can be seen, the efficiency does not differ greatly when the frequency varies. Small differences are due to the fact that less active power is on the output when the frequency increases. Moreover, at high frequencies the CCSC can be enabled in order to improve efficiency, specially at high modulation indexes.

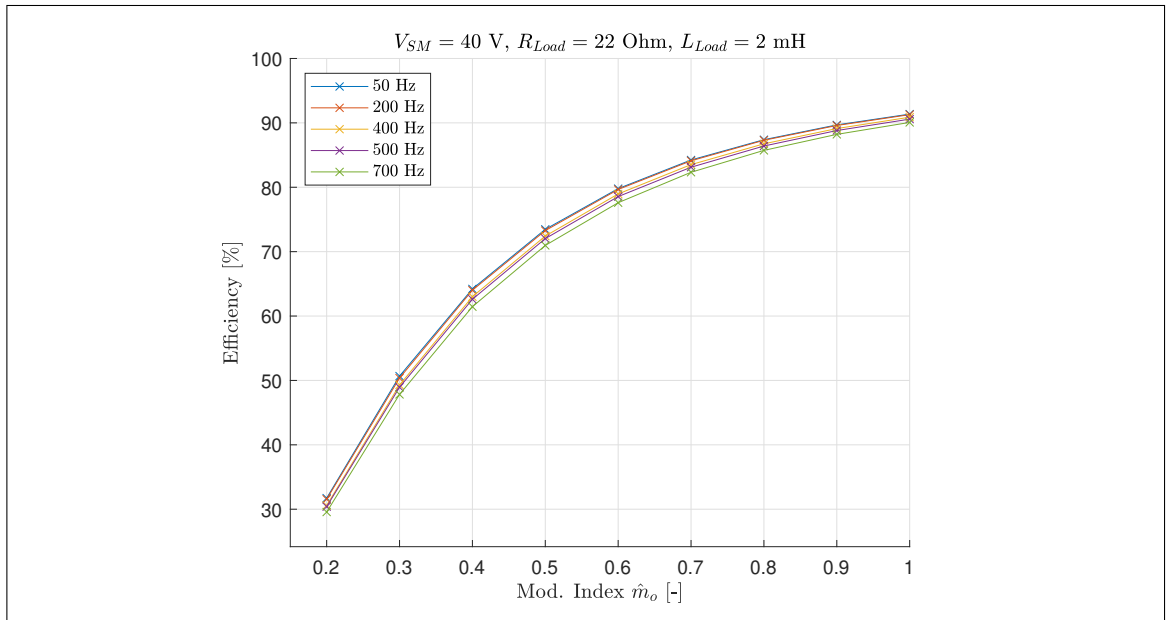


Figure 6.15. Efficiency as function of modulation index for different fundamental frequencies (CCSC disabled).

The previous curve does not consider a high load, but a similar behavior is extended to different loads, depending on the ratio of the resistance and reactance of the load. Figure 6.16 shows the efficiency as function of the modulation index for different loads at 50 Hz. With higher loads (lower R_{Load}) the efficiency increases accordingly. As mentioned previously, it must be remembered that different aspects of the prototype can be improved so the efficiency can increase. But the main purpose of obtaining this curve is that the efficiency can reach higher values when the loads increases. In the Figure, the increase in efficiency between $R_{Load} = 11 \Omega$ and $R_{Load} = 7.3 \Omega$ is not that significant but only because the reduction of the load resistance is small. If a lower resistances were used,

then the increase in efficiency would be more notorious. The curves with higher power are above 94% of efficiency at full modulation index. The maximum registered efficiency in all the performed tests was $\eta = 94.23\%$, at $V_{SM} = 60$ V, $f_0 = 50$ Hz and full modulation index.

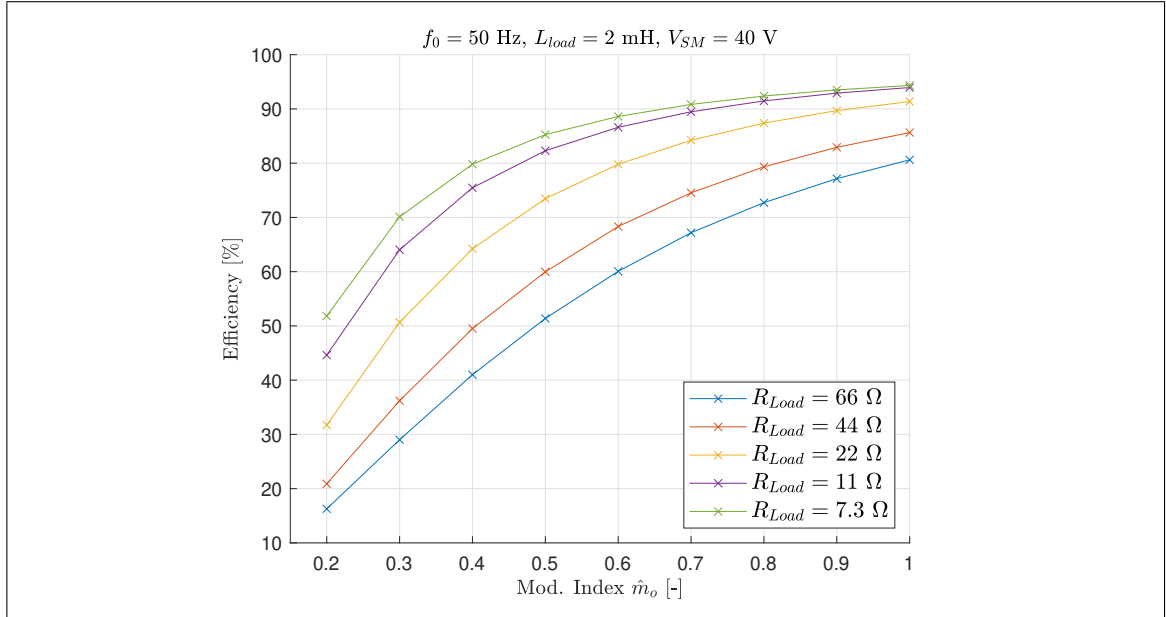


Figure 6.16. Efficiency as function of modulation index for different loads (CCSC disabled).

The reason of the increase in efficiency is due to the fact that low-voltage high-current MOSFETs are used in the converter. Although the number of semi-conductor is high, their on-state resistance is considerably low and therefore the conduction losses do not increase excessively when the current rises. The rise in power is greater than the increase of the conduction losses, even when the latter depends quadratically on the driven current. The majority of the losses of the converter comes from the switching losses due to the high switching frequencies involved, specially on the DAB H-Bridges. The switching losses, in a simplified manner, depend quadratically on the semi-conductor voltage and it is common for them to be the main source of losses in different converters. In other conditions, the voltage ripple would increase notoriously when the converter drives a

greater output power, but thanks to the active work of the DAB this does not happen in the ALE-MMC. This allows to maintain the switching losses relatively constant, or at least the factor that depends on the semi-conductor voltage, since these losses depend in a more complex way on the driven current.

Summarizing, the converter can achieve greater efficiencies given the conditions. The curves could reach above 94% of efficiency even when the developed prototype was not optimized, which includes the absence of cooling system, limited dead-times and current limitation due to laboratory conditions. Also, the maximum reached power was not specially high, so the full power behavior of the converter could not be observed. Nevertheless, the obtained curves show that there is a tendency for the converter to increase the efficiency when the output power becomes higher. Obviously, this increase will be limited and different when temperatures become higher, where a cooling system may be needed in order to maintain a proper performance and conditions. As said before, as the losses are distributed in a large number of devices, the cooling system may also be simple.

7. CONCLUSIONS AND FUTURE WORK

In **Chapter 4** a mathematical model for the ALE-MMC was developed using the models and equations from the previous chapters so the operation of the DAB could be determined, since it is the main feature of the topology. A major result from this analysis is that the DAB RMS current will depend on the arms modulation indices and currents, and in the worst case it will handle less than 18% of the converter output RMS current. Then, the power it will handle will depend on the number of SMs used in the converter given a DC-link voltage. Moreover, no voltage sensors in the SMs are needed for the operation, so the converter measurement system can be greatly simplified.

In **Chapter 5**, a three-phase converter simulations were presented in order to verify the developed theory, driving 5.6 kVA of power to an RL load. In normal operation and low frequency, the converter achieved less than 1% of SM voltage ripple with respect to its DC value. This, even with a capacitance as low as 220 μF , an output current of 25 A peak, and without any voltage control or balancing methods. This demonstrated the effectiveness of the DABs for handling the power ripple. On the other hand, as the frequency increased and approaches the circulating current resonance range, the SMs power ripple increase accordingly, reaching a 10% of amplitude respect to the DC value, but still it had a stable operation.

Regarding the circulating current suppression, results showed that enabling the suppression at low frequencies lead to a SMs voltage ripple of almost 20% with respect to the nominal DC-value, but the converter variables did not diverge and the converter did not destabilize. On the other hand, at higher frequencies the circulating current suppression did decreased the voltage ripple to about 5% of the DC value, and greatly reduced the RMS value of the circulating current, given the closeness to the resonance range. This confirms that the circulating current control should be used in higher frequencies (and close to the resonance range) to improve the performance, while in low frequencies it is not recommended. With this consideration, the simulations showed that the SMs voltage

ripple can be maintained less than 5% of the nominal DC value for the entire operating frequency range, given a constant output current.

Another important result is the capability of driving the nominal output current at zero-frequency conditions. The converter can drive DC power to the load without any additional control logic or current injections, with a SM voltage ripple of less than 1% of the DC value. It is actually a condition where the DABs have their maximum performance given the DC behavior of the variables. If compared to the classical MMC topology, where current injection is needed, in the ALE-MMC the components do not need to be sized for higher currents for operating in DC conditions, thanks to the DAB function.

In the simulations, the estimation for the DAB current was validated, where it was seen that the DAB handled about a 14% of the converter output current with the CCSC enabled. This fitted with the values predicted in **Chapter 4**, and thus can be used for designing and sizing the components for the DAB. Moreover, given that it will drive always less than 18% of the output current, the DABs H-Bridges can make use of lower current-rated devices in order to save costs.

For an initial notion of the converter efficiency, the losses of the switching devices of the ALE-MMC were modeled, considering 100 V and 300 A MOSFETs. For an output current of 25 A (5.6 kVA), at lower frequencies the converter had lower losses with the CCSC disabled, having a difference of about 100 W between both cases. On the other hand, at higher frequencies the converter had lower losses with the CCSC enabled, showing a difference of more than 200 W of losses. Also, the ALE-MMC semiconductors losses (at 1 kHz SM switching frequency) were compared with a Two-Level inverter (with 600 V and 109 A MOSFETs, 10 kHz switching frequency), where the Two-Level inverter presented 696 W of estimated losses with 5.99 % of output current THD, in contrast of the 444 W of losses and 1.09 % THD of the ALE-MMC. At a first glance, the ALE-MMC seems superior. However, in order to give an accurate statement, the DABs transformer losses must be taken into account, which is an analysis proposed for future works.

Finally, **Chapter 6** presented the experimental results performed with a single-phase low scale prototype. The converter behavior was very similar to the one in the simulation and thus matched the theoretical analysis.

Normal operation test with a 270 μF SM capacitance, gave a voltage ripple of 3 % around the DC value at low frequencies (50 and 250 Hz, 9.5 A output current), and around 7.5 % for higher frequencies (500 and 700 Hz, 8 A output current). The behavior was the expected from the simulation results, so the converter operation and principles were validated experimentally, and the DAB accomplishes its main purpose.

Test regarding the circulating current suppression were performed, and the results also matched the simulations behavior. With 7 A of output current and 100 Hz, the SM voltage ripple increased from 2 % to 10 % when the CCSC was enabled, reducing the general performance of the converter. At an output current of 7.5 A and 700 Hz the SM voltage ripple was reduced from 6.5 % to 4 % when the CCSC was enabled, increasing the performance. Furthermore, the CCSC at 700 Hz translated into an increase of 0.865 % in the converter efficiency and a decrease of 0.65 % on the output current THD. Contrary, at 100 Hz the CCSC decreased the efficiency by 0.535 %, and increased the THD by 3.1 %. These results confirm that the CCSC should be enabled at higher frequencies, where it does increase the DAB performance and increase the efficiency of the converter, and even reducing the voltage ripple. On the other hand, at low frequencies it is convenient to let flow the AC circulating current in order to help the balancing of the capacitors.

A transient test on the converter showed that when approaching to the center of the circulating current resonance range, the current reached twice its value compared to the case without resonance, while driving the same 5.8 A of output current in the frequency ramp. This increase was expected, and even affects the SMs voltages. With the CCSC enabled before entering the resonance range, the converter can inhibit its effects and a voltage ripple less than 5 % of the nominal value can be reached in the frequency transient.

Concluding the experimental results, the efficiency of the converter was studied. A high current test was performed in an attempt to obtain a relative high power in the low scale converter, reaching 1.1 kW (17 A of output current) of power with a voltage ripple of 3.5 % with respect to the DC value. An efficiency of 94.062 % was achieved, and considering the symmetry of the legs in the converter, the same efficiency can be expected for a three-phase converter driving 3.3 kW of power in the same conditions. The maximum efficiency registered was 94.23 %, with a DC-link of 240 V and full modulation index. Due to laboratory limitations, higher powers could not be reached, but efficiency vs. modulation index curves at different loads (and same DC-link) were obtained. The tendency in the curves imply that the converter increases the efficiency as the load increases, and thus efficiencies higher than 94.23 % can securely be expected.

As an overall conclusion of the developed work, the results confirm the hypothesis of this thesis. The converter principles worked and the performance is as expected from a classical MMC topology and control, logically, considering the major differences. An operation with greatly reduced capacitance was achieved, and waveforms such as SM voltage ripple and output current presented a good quality. A 94.23 % of efficiency was achieved, which is a good and reasonable value for a low scale prototype, but the data obtained shows that the converter can reach even higher efficiencies given proper conditions. And least, a proper logic of the CCSC allows to get maximum performance on the operating frequency range, where the suppression at high frequencies improves the overall performance.

Finally, this work served as an initial validation for the ALE-MMC and its usage on low voltage and variable frequency applications. It validated the converter operation, where it can operate from zero-frequency to high frequencies with good performance and with a simplified control logic, confirmed by both simulation and experimental results. Thus, this opens the way for future works to extend the scopes of the experiments using a full-power three-phase converter and improving different issues such as dead-times, components limitation, etc, and making full analysis on the DAB efficiency and core

losses. Then, a reliable comparison can be made with actual solutions for these applications, focusing on the benefits of modularity and power quality that the ALE-MMC brings to the low-voltage range.

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